An Improved Input Test Pattern for Characterization of Full Adder Circuits

Manan Mewada, Mazad Zaveri

Department of Information and Communication Technology, IET, Ahmedabad University, India

***Abstract*—Full Adder is an important circuit block of many digital CMOS VLSI sub-systems, and its performance is input dependent. Input test patterns play a crucial role in the characterization and analysis of any circuit, including: measurement of propagation delay and estimation of power dissipation, and functional verification. Input pattern proposed in this paper, include all 56 possible transitions, including the transitions that lead to maximum propagation delay. This pattern also provides a fair estimate of the power dissipation, and is also suitable for functional verification. The proposed input pattern is applied to different full adder circuits (spice simulation using 45 nm MOSFET models). The results show that the proposed input pattern provides comparable/correct estimates of propagation delay and power dissipation, using less number of input transitions as compared to other patterns reported earlier.**

Keywords*—*Full adder, Characterization, Input test pattern, Propagation delay, Power dissipation, Functional verification

I. INTRODUCTION

Addition is one of the basic arithmetic operations, which is widely used in many digital CMOS VLSI systems, such as: micro-processors, DSP processors, GPU, etc. The basic building block of a multi-bit adder is the Full Adder (FA). Apart from the addition operation, FA is also used in other operations, such as: subtraction, multiplication, address generation, etc. In all these operations, the FA generally falls into the critical path of the system, and hence, the overall performance of the system is affected by the performance of the FA.

Several CMOS VLSI circuits/implementations have been suggested for FAs [1-8] (shown in Fig. 1-7), primarily to improve the performance, and to explore the trade-offs in terms of propagation delay, power dissipation, and driving capacity. However, many of these circuits/implementations [1-8] were characterized using some basic input pattern(s), which lacked important transitions that capture maximum propagation delay, and provide a fair estimate for power dissipation. Some previous work [9] has attempted to solve these limitations, by improving the input pattern(s); however, these input patterns contain a large number of input transitions (more than 56 transitions).

In this paper, we propose an input pattern for FA, that can measure maximum propagation delay, estimate fair power dissipation, and verify the correct functionality, using only half the number of input transitions as compared to input pattern form [9].The rest of this paper is organized as follow; section 2 discusses the qualities required in input test pattern to characterize the FA. Section 3 provides our proposed input pattern. In section 4, we compare results obtained for our proposed input pattern with previously published work [9].

II. QUALITIES OF GOOD FULL ADDER

A good test pattern should satisfy the following: (1) Capture the maximum propagation delay (2) Provide a fair estimate of power dissipation, and (3) Correct functionality.

(1) Maximum propagation delay

The propagation delay of a cell is defined as the time from 50% of input[1] voltage swing to 50% of output[2] voltage swing [2]. [Note: A cell means a digital circuit block with multiple inputs and multiple outputs, generally consisting of more than one standard or compound gate.] A FA cell, will consist of three inputs {A, B, Cin} and two outputs {Sum, Cout}. Cell delay is dependent on the previous value and the current value of the (binary) inputs, because of the pre-charging/pre-discharging of intermediate nodes of the gates during the previous value [9]. For the FA, there are total 8 different possibilities for both, previous value and current value of inputs {A, B, Cin}. Hence, there are total 64 possible transitions (from previous value to current value of inputs). For example, {000} (previous) to {000} (current), {000} to {001}, {000} to {002} and so on. Among these 64, only 44 are useful for measuring propagation delay. Maximum propagation delay will occur for one or more of these 44 transitions. Transitions, such as {000} to {000}, {010} to {100}, {110} to {101}, etc., which do not cause any change in the outputs, are not useful[3] when measuring propagation delay. A good test pattern should include the useful 44 transitions.

(2) Power Dissipation

Power dissipation is defined as the rate at which energy is drawn from the supply. To estimate fair power dissipation, input pattern should be chosen carefully. In good test pattern higher frequency should alternate at all inputs by ensuring

1If there are more than one inputs in a cell, then the first input that reaches 50% voltage swing should be considered.

2 If there are more than one outputs in a cell, then the last output that reaches 50% voltage swing should be considered.

3 Note that, some of these transitions (where the output does not change), can still consume switching power because the intermediate nodes and intermediate outputs in the cell may change.

equal number of high to low and low to high transitions (at each of the inputs). One example of bad test pattern is shown in fig. 9, here input A is fluctuating at higher frequency than inputs B and Cin, this may not occur in real situation, and it may lead to wrong estimation of power dissipation. Input pattern should also contain input transitions for which inputs are changing but the outputs are not necessarily changing. Such transitions can be used to investigate and estimate the power dissipation due to switching of internal nodes and outputs of a cell. Again considering the same example pattern of fig. 9, for any input combination, output is changing. So, it's not easy to capture internal switching power dissipation.

(3) Functional Verification

Functional verification of the FA could be defined as the correct generation of (outputs) Sum and Carryout for given inputs, with proper driving capacity (for practical loading conditions). Incorrect (settled voltage levels) or sluggish outputs may be generated due to faulty layout or due to under-sizing of the transistors. Input pattern should also verify the correct functionality of FA.

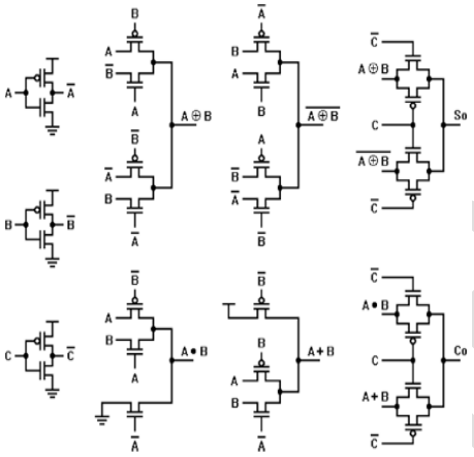

Fig.1 Moriano ours1 full adder [1]

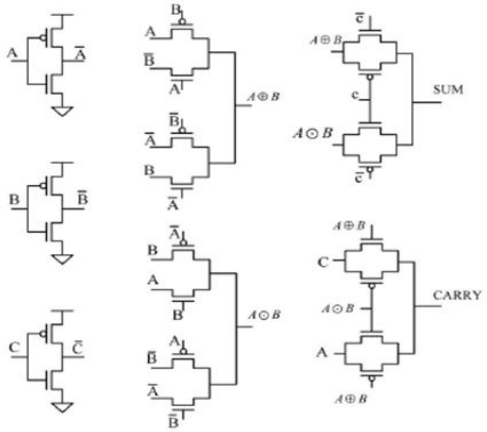

Fig.2 Hybrid CMOS1 full adder [6]

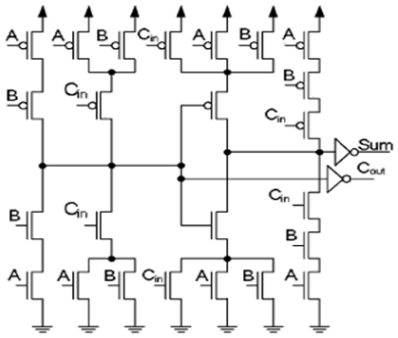

Fig.3 28T Mirror CMOS full adder [3]

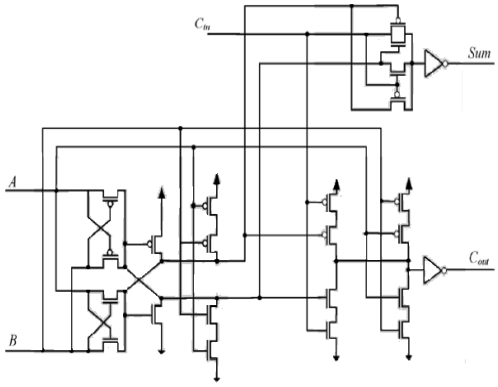

Fig.4 New HPSC adder [2]

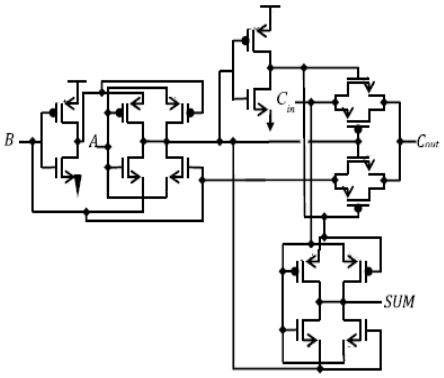

Fig.5 Hybrid CMOS2 full adder [4]

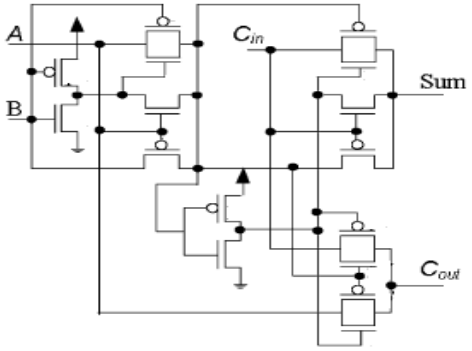

Fig.6 TFA full adder [5]

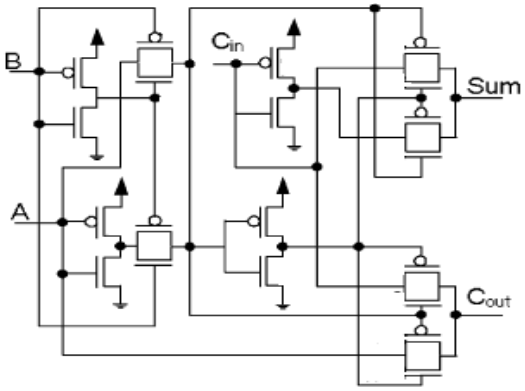

Fig.7 TG CMOS full adder [5]

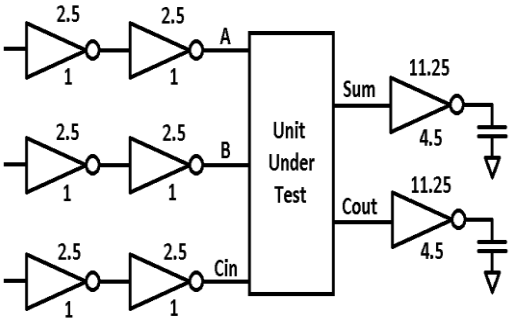

Fig.8 Test bed used for Simulation [7]

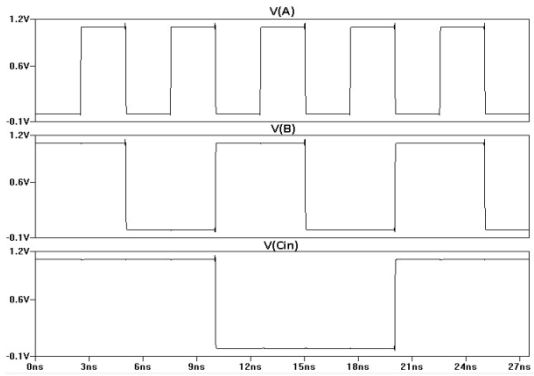

Fig. 9 Example of bad test pattern

III. PROPOSED INPUT PATTERN

Our proposed input pattern (with 56 input transitions) is shown in fig. 10. All 44 input transitions needed for measuring propagation delay are covered in our proposed input pattern. Also all the inputs are introduced to higher frequency with equal number of high to low and low to high transitions, total number of transitions at each input is 32. Proposed input pattern also contains the remaining 12 input transitions for which inputs are changing but outputs are not changing (which can capture internal switching power dissipation). Total 56 input combinations are enough to verify the correct functionality of FA.

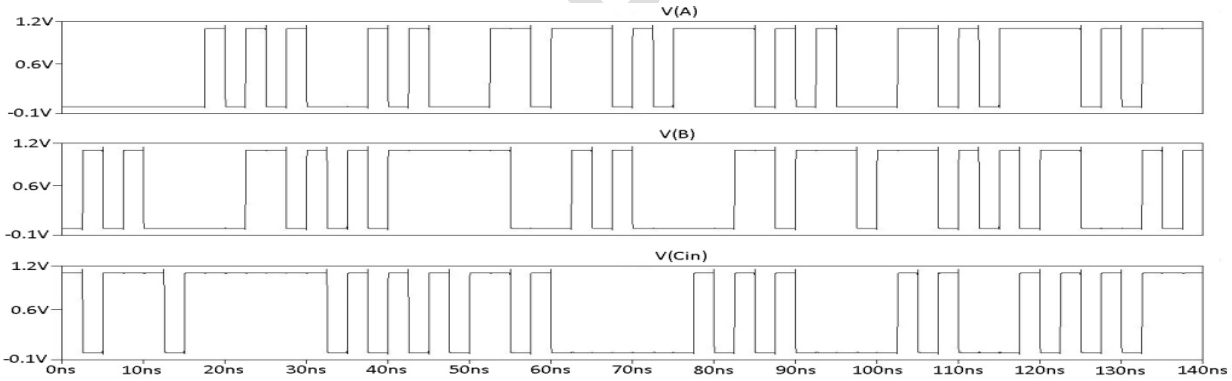

Fig.10 Proposed input pattern

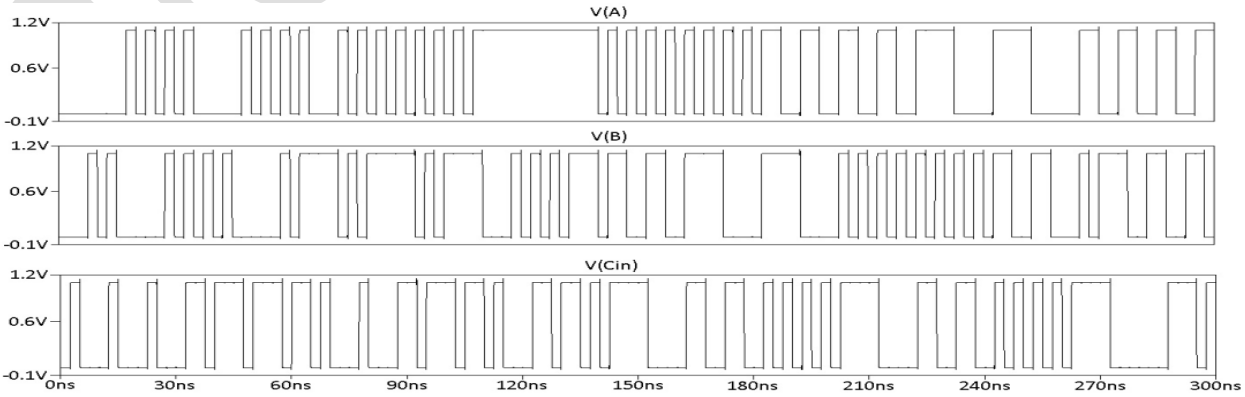

Fig.11 Pattern suggested in [9]

Table 1:Propagation Delay Simulation Results. Unit Is Ps

Adder		Pattern from [9]	Maximum propagation delay transition for Pattern from [9]	Proposed pattern	Maximum propagation delay transition for proposed pattern	Bad input pattern [9]	Maximum propagation delay transition for bad input pattern
Moriano ours1 [1]	Sum	245	011->001	245	011->001	221	101->010
	Carry	230	001->110	230	001->110	212	010->110
Hybrid CMOS1 [6]	Sum	240	110->010	240	110->010	214	101->010
	Carry	214	101->100->110	215	001->100->110	208	010->110
28T Mirror [3]	Sum	234	110->010	234	110->010	219	101->010
	Carry	165	101->001->110	164	000->001->110	163	010->110
Hybrid CMOS2 [4]	Sum	280	110->100	280	110->100	253	000->100
	Carry	278	011->001	278	011->001	228	001->101
New HPSC [2]	Sum	255	101->001	255	101->001	219	010->110
	Carry	180	001->111->010	181	100->111->010	154	001->101
TFA [5]	Sum	248	110->100	248	110->100	231	000->100
	Carry	203	100->110	203	100->110	189	010->110
TG CMOS [5]	Sum	201	110->010	201	110->010	169	011->111
	Carry	165	001->011	165	001->011	164	010->110

Table 2.Power Dissipation Simulation Results. Unit Is Uw

Adder	Pattern from [9]	Proposed Pattern	Difference in %
Moriano ours1 [1]	11.355	11.170	1.66
Hybrid CMOS1 [6]	10.578	10.329	2.40
28T Mirror [3]	10.024	9.733	3.01
New HPSC [2]	9.167	8.929	2.65
Hybrid CMOS2 [4]	12.696	12.351	2.38
TFA [5]	10.357	10.184	1.70
TG CMOS [5]	10.862	10.680	1.70

IV. SIMULATION RESULTS AND CONCLUSION

Our proposed input pattern is compared with other input patterns [9], in terms of their ability to capture maximum propagation delay, estimation of power dissipation, and the number of input transitions in the pattern. Among all other patterns [9] [10], we found that input pattern introduced in [9] (shown in fig. 11) is comparable with our proposed input pattern (shown in fig. 10). Both these patterns are applied to seven different FA circuits [1-6] (shown in fig 1-7) and results were compared. All the FA circuits are designed and simulated in LTspice using BSIMv4 45 nm model (level = 54). Maximum frequency of the inputs is 200 MHz. Test bed used for simulation is shown in fig. 8 [7].

Table 1, shows the maximum propagation delay, measured by our proposed input pattern and input pattern from [9]. Results are nearly identical; a minor difference in results of the pattern for some adder is due to previously trapped charges (from the previous-to-previous input transition). In table 2, power dissipation results are shown. We have provided power dissipation, averaged over input pattern (all transitions). Estimates of power dissipation for input pattern from [9] is (1.6% to 3%) higher than the estimated power dissipation for our proposed input pattern. The maximum difference is 3%. The difference in the estimated power, is due to the fact that input pattern form [9] contains 64 transitions (last 64 transitions out of the 120 transitions shown in fig.11), just for the sole purpose of estimating power dissipation, whereas our proposed input pattern contains in all only 56 transitions. Comparing two patterns with respect to number of input combinations is showing that input pattern form [9] contains total 120 input transitions, while our proposed input pattern contains 56 input transitions. Our proposed input pattern can measure maximum propagation delay, estimate fair power dissipation, and verify the correct functionality, using only half the number of input transitions as compared to input pattern form

REFERENCES

[1]. Mariano Aguirre, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications", IEEE Transactions On VLSI Systems, Vol. 19, No. 4, April 2011.

[2]. Chip-Hong Chang, "A review of 0.18-um full adder performances for tree structured arithmetic circuits", IEEE Transactions On VLSI Systems, Vol. 13, No. 6, June 2005.

[3]. Reto Zimmermann, "Low-power logic styles CMOS versus pass-transistor logic", IEEE Journal of Solid-State Circuits, Vol. 32, No. 7, July 1997.

[4]. Partha Bhattacharyya, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit", IEEE Transactions On VLSI Systems, Vol. 23, No. 10, December 2014.

[5]. Ahmed Shams, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells", IEEE Transactions On VLSI Systems, Vol. 10, No. 1 February 2002.

[6]. Narasimha Rao, "Power Aware and Delay Efficient Hybrid CMOS Full-Adder for Ultra Deep Submicron Technology", 2013 European Modeling Symposium (ESM), November 2013.

[7]. SumeerGoel, "Design of Robust, Energy-Efficient Full Adders for Deep Submicrometer Design Using Hybrid-CMOS Logic Style", IEEE Transactions On VLSI Systems, Vol. 14, No. 12, December 2006.

[8]. Nan Zhuang, "A New Design of the CMOS Full Adder", IEEE Journal of Solid-State Circuits, Vol. 27, No. 5, May 1992.

[9]. A.Shams, "Performance Evaluation of 1 bit CMOS Adder Cells", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Vol. 1, Jul 1999.

[10]. Callaway, "Estimating the Power Consumption of CMOS Adder", Computer Arithmetic, 1993. Proceedings., 11th Symposium on, 1993.

[11]. Mariano Aguirre, " An alternative logic approach to implement high-speed low-power full adder cells", ACM 18th annual symposium on Integrated circuits and system design, September 2005.

[12]. Massimo Alioto, "Analysis and Comparison on Full Adder Block in Submicron Technology", IEEE Transactions On VLSI Systems, Vol. 10, No. 6, December 2002.

[13]. Mingvan Zhang, "A novel hybrid pass logic with static CMOS output drive full-adder cell", Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on, Vol. 5, 2003.
[14]. S. Agarwal, "Energy Efficient High Performance Circuits for Arithmetic Units", 21st International Conference on VLSI Design, 2008.
[15]. ShekharVerma, "New High Performance 1-Bit Full Adder Using Domino Logic", 2014 Sixth International Conference on Computational Intelligence and Communication Networks, 2014.
[16]. V. Agrawal, "Essential of Electronic Testing", Kluwer Academic Publishers, 2002, Ch. 5.
[17]. N. Weste, "Principles of CMOS VLSI Design", Addison-Wesley, 1988, Ch. 5.
[18]. Kiat-Seng, "Low Voltage, Low Power VLSI Subsystems", Tata McGraw Hill Edition, 2009.