Architecture for an Efficient Memory Built in Self Test

Nisha O. S.[#1], Dr. K. Siva Sankar[*2]

[#1]*IT Department, Lourdes Matha College of Science and Technology, Trivandrum, India-695574*

[*2] *IT Department, Nooral Islam University, Nagercoil, India-629180*

***Abstract*: Today's submicron VLSI technology has been emerged as integration of many VLSI ICs into a single Si Chip called System-on-Chip (SoC). The SoC architecture normally contains multiple processors along with either separate or centralized memory blocks as its core elements as well as many noncore elements. Embedded RAMs are those whose address, data, and read/write controls cannot be directly controlled or observed through the chip's 1/0 pins. Testing these memories, which are incorporated on a large percentage of VLSI devices are harder just because of the lack of controllability of its inputs and observe ability of its outputs. Testing such RAMs is the main objective of this paper. It is challenging to test embedded RAMs, and hence we will discuss techniques - design for testability (DFT) and built-in self test (BIST), which help in improving the testability of these RAMs.**

***Keywords*- Built-In Self Test (BIST), March algorithm, Switching factor.**

I. INTRODUCTION WITH MOTIVATION

Today's semiconductor technology is making it feasible to integrate millions to billions of circuit elements e.g., diodes, transistors and other components such as resistors and capacitors, together with interconnections, within a very small Silicon area [1]. The shrinking of technology has created various mechanical and physical defects such as opens, bridges and shorts causing more parasitic capacitances, leakage power and their severe effects on the overall performance of the System-on-Chips (SoCs). Earlier, the SoCs were influenced by its functional cores, but because of the increased demand of high data storage, SoC area is currently being influenced by the on-chip Volatile or Non-volatile memory blocks [2], [3]. As a result of the survey made by Semiconductor Industry Association (SIA), the semiconductor memories are expected to occupy 94% of SoC area in 2014 as compared to 71% in 2005.The user data will be generally stored in volatile SRAM, whereas the nonvolatile ROMs store the system programs as well as the test program and test vectors by which the system will be tested for any manufacturing defects and functional errors during test mode [4]. The exact functionality of the memory chips is becoming vital in SoCs, because the control data/signals used for controlling and functioning of almost all the blocks in SoCs, their scheduling information in addition to the user data are being stored on-chip to reduce the latency as compared to that of storage of these data in an off-chip storage device.

The most commonly occurring functional faults [5], [6] in regular 2D memory arrays include Address decoder Faults (AFs), Stuck-At Faults (SAFs), Neighborhood Pattern Sensitive Faults (NPSFs) and Coupling Faults (CFs). As the memories in SoCs are mostly occupying the higher chip area, the study and application of fault models that can target these memory faults has become significant for cost effective memory testing. Unlike the logic blocks, the memory arrays have an identical 2-dimensinal structures, the MBIST algorithms may be commonly applied for testing of all memory arrays available in SoCs. The memory can be effectively tested using march algorithms [7], [8].

Power dissipation is becoming a challenging problem for the VLSI design engineers and testing engineers because the power consumed by the system in testing mode is 200% more than in its normal mode [9]. There are two types of power dissipation 1. Static power 2. Dynamic power and in this case we are going to consider the dynamic power dissipation .The dynamic power dissipation is calculated from an equation

$$P_{avg} = \alpha T C_{load} V_{dd}^2 f_{clk} \quad (1)$$

Where,

αT -Switching activity factor of the gate.

C_{load} -Total load capacitance

V_{dd} -Supply voltage

f_{clk} -Operating frequency

In the above equation the average power is directly proportional to the 'αT'. Therefore the power dissipation

during testing can be reduced by controlling the switching activity .The advancement in submicron manufacturing technology and system-on-a-chip (SOC) design methodology has led to a large number of cores, especially the memory cores, are now integrated into a single chip. It has been predicted that by the year of 2014, memory cores may occupy 94% area of a typical SOC [10]. Memory thus plays an important role in SOC. Since the probability of memory fault is more compared to that of other type of faults in a circuit the need for testing of memory is more important. However due to the availability of a small number of I/O pins in a circuit BIST for Memory (MBIST) is used as a solution to this problem [11].In conventional MBIST the address bus, data bus, and read/write control signals that are generated by the test pattern generator of the BIST are applied to the memory under test. The address bus indicates the memory location, the Read/write control determines the operation (read/write) to perform in this particular memory location and the data bus include the data to write or to read in the memory location the address bus indicate.

II. RELATED WORKS

K. Murali Krishna and M. Sailaja in [12] implemented an LFSR based address generator with reduction in switching activity for low power MBIST. In that method the address patterns were generated by a combination of LFSR and a 2-bit pattern generator (Modified LFSR) and two separate clock signals. By using the modified architecture switching activity was reduced. Since the switching activity was proportional to the power consumed, reducing the switching activity of the address generator reduces the power consumption of the MBIST. They had designed and stimulated their address generator using Xilinx ISE tools and compared with the switching activities of the conventional LFSR and BS-LFSR. Results showed a reduction in switching activity and a reduction of more than 90% of the total dynamic power when compared to conventional LFSR.

Balwinder Singh *et.al* in [13] implemented all March algorithms used for memory testing in verilog for the testing of 1Kb and 4kbmemories with BIST. After designing and implementation, their performance is compared on the basis of their length, number of cycles used during writing and reading of memory, and area overhead. All that comparison was presented in the tabular form. From comparison on the basis of area overhead, it is observed that for the memories of smaller in size March X is most efficient and March AB is the least efficient, and Vice versa in the case of March Y and March LA . During the analysis power consumption it was examined that March X and March C consume least power in case of 1 Kb memory and 4 Kb memories respectively. March C, X and Y takes the least number of cycles for memory writing and reading in 1Kbmemory and March Y in case of 4 Kb memory.

Che-Wei Chou *et.al* in [14] presented a low-cost built-in self-diagnosis (BISD) scheme for NAND flash memories, which could support the March-like test algorithms with page-oriented data backgrounds. Two simple test time reduction techniques were also designed to reduce the test time. Experimental results showed that the proposed BISD circuit for a 2M-bit flash memory only needs 1.7K gates. Also, their new test time reduction techniques could effectively reduce the test time. Analysis results showed that they can reduce the test time to 48.628% of the normal test scheme for a 4G-bit flash memory tested by the March-FT test algorithm with solid data backgrounds.

A systematic approach in testing flash memories, including the development of March-like test algorithms, cost effective fault diagnosis methodology, and built-in self-test (BIST)scheme was presented in [15] by Jen-Chieh Yeh *et.al* . The improved March-like tests algorithms can detect disturb faults derived from the IEEE STD 1005 and conventional faults. As the memory array architecture and/or cell structure varies, the targeted fault set may change. They have developed a flash-memory fault simulator called RAMSES-FT, with which they could easily analyze and verify the coverage of targeted faults under any given test algorithm. In addition, the RAM test algorithm generator test algorithm generator by simulation has been enhanced based on RAMSES-FT, so that one can easily generate tests for flash memories, whether they are bit- or word-oriented. Their newly designed fault diagnosis methodology helps improve the production yield. They also developed a built-in self-diagnosis (BISD) scheme a BIST design with diagnosis support. The BISD circuit collects useful test information for off-chip diagnostic analysis. It had unique test mode control that reduces test time and diagnostic data shift-out cycles by a parallel shift-out mechanism.

In [16] Masnita et.al, had designed a data and read/write controller as a finite state machine (FSM) BIST that would generate test patterns based on the march-based diagnostic algorithm developed to distinguish between stuck-at and transition faults. A description related to SAFs and TFs were presented with the intention of covering the aspect of distinguishing both of these faults. Related design based on the selected algorithm was also presented with simulation results to show the functionality of the design. The design of the controller can be used to build a complete MBIST engine to test the effectiveness of the proposed algorithm in distinguishing SAFs from TFs.

Manikandan.B and Praveen kumar.J implemented a FSM-based programmable memory built in self test (MBIST) Controller used for testing the memory devices in [17]. The MBIST controller was designed to implement a new test algorithm known as March based test algorithm. The controller and test algorithm are studied and designed using verilog HDL and implemented in SPARTAN-3E FPGA. The simulation portrays that the tested data and the expected data

are able to be compared in the architecture. The implemented controller has the ability to detect faulty or good memory ICs. Synthesis result shows that the FSM -based HP-MBIST controller employed only 75 instances with clock frequency 246.15 MHz with a less usage of Logic Elements (LE) with High speed testing of memories. It was also justified that the FSM-based HP-MBIST controller consumes less area overhead and high speed while the other compared designs consumed more area overhead and less speed. The experimental results also showed that the presented BIST can be implemented with low area overhead.

K Padma Priya in [18] presented a high speed FSM-based controller for programmable memory built-in self test for testing memory devices. Her technique was popular because of its flexibility of new test algorithms. The architecture of controller was designed to implement a new test algorithm has less number of operations and the designed algorithm emphasis testing of high density memory ICs either faulty or good .The components of controller was analyzed and designed using Verilog HDL. The analysis of the timing, logic area usage and speed are also presented.

In [19] M. Jahnavi *et.al*. Presented the implementation of online test scheme for RFID memories based on Memory Built in Self Test (MBIST) architecture. In that work they presented the, Symmetric transparent version of March SS algorithm, implementation of Memory BIST. The comparison between the different march algorithms and the advantage of the March SS algorithm over all other is also presented. The whole design was implemented using Verilog HDL and was, in turn, verified on Xilinx ISE 13.2 simulator, and synthesized.

III. RESEARCH METHODOLOGY

The test algorithm and address generation are to be optimized to cover all the faults, reduce testing time and consume less power. This can be achieved by employing evolutionary algorithms in selecting the patterns such that the inputs of design switch minimally. Test algorithm is designed using these evolutionary algorithms so that the test vectors selected can be used for reducing the switching activity in the circuit and also by maintain the fault coverage. Considering the above facts, in this work I have planned to implement a highly efficient MBIST architecture. Since the main source of power and area consumption of the whole system is dependent on the address generator and the test algorithm used in the MBIST architecture, I have planned to use an LFSR based address generator with low switching activity [11] with modification for its operations based on the adapted testing algorithm. After analyzing the Area Overhead and Power Analysis of March Algorithms for Memory BIST [12] it is obvious that the MARCH-Y algorithm requires low area and power with less clock cycle for its operation, So in this work for better result I have planned to analyze the drawbacks of that algorithm and to modify the algorithm for efficient contribution. The MBIST controller can be designed using a FSM with better state transition.

IV. CONCLUSION

The literature survey revealed that a lot of researches have gone in this area for a low powerconsumption system. This paper presents a methodology for memory testing. Another peculiarity ofthis paper is the introduction of a test mechanisms to improve the reliability and performance of SoCs due to technology miniaturization and increased memory density, there is a need to incorporateon-chip self-testing unit for testing these memory units. Most recent research areas trying toincorporate all the techniques described in this paper to make a perfect architecture for an efficientmemory built in self-test.

REFERENCE

[1]. Kiran Gupta and T R.Gopalakrishnan.Nair , "A Study of VLSI Technology, Wafers and Impact on Nanotechnology", IEEE National Conference on Advanced VLSI/DSP, Bangalore, 2008.

[2]. David Choi, Kyu Choi, and John D. Villasenor, "New Non-Volatile Memory Structures for FPGA Architectures", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 7, July 2008.

[3]. Technical report on "Non-Volatile Memory: Emerging Technologies And their Impacts on Memory Systems "Porto Alegre, Sep 2010.

[4]. Venkatapathi Naidu Rayapati, "VLSI semiconductor random access memory functional testing", Microelectronics Reliability, Vol.30, No 5, pp: 877–889, 1990.

[5]. R. Dekker, F. Beenker, A. Thijssen, "Fault modeling and test algorithm development for static random access memories," International Test Conference 1988.

[6]. D. Niggemeyer, M. Redeker, J. Otterstedt, "Integration of nonclassical faults in standard march tests," International Test Conference 1998, pp. 91-6.

[7]. S. Hamdioui, A. J. van de Goor, and M. Rodgers, "March SS: A test for all static simple RAM faults," in *Proc. IEEE Workshop MTDT, Jul.* 2002, pp. 95–100.

[8]. L. Dilillo, P. Girard, S. Pravossoudovitch, and A. Virazel, "Dynamic read destructive fault in embedded-SRAMs: Analysis and March test solution," in *Proc. IEEE Eur. Test Symp., May 2004, pp. 140–145.*

[9]. Luca Benini, Member, Alessandro Bogliolo, and Giovanni De Micheli, "A Survey of Design Techniques for System-Level Dynamic Power Management," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000.

[10]. E. J. Marinissen, B. Prince, D. Keitel-Schulz, Y. Zorian, "Challenges in Embedded Memory Design and Test", Proc. of Design, Automation and Test in Europe, 2005, pp. 722 – 727.

[11]. NurQ.Noor, YusrinaYusof, and AzilahSparon, "Low Area FSM-Based Memory BIST for Synchronous SRAM", proceeding of the international colloquium of Signal Processing and Its application, 2009, pp. 409-412.

[12]. K. Murali Krishna and M. Sailaja, "Low Power Memory Built in Self Test Address Generator Using Clock Controlled Linear Feedback Shift Registers", Journal of Electronic Testing, Theory and Applications (JETTA), Vol.30, No.1, pp: 77-85, Feb.2014.

[13]. Balwinder Singh, Arun Khosla and Sukhleen Bindra Narang, "Area Overhead and Power Analysis of March Algorithms for

Memory BIST", International Conference on Communication Technology and System Design, pp: 930 – 936, 2012.

[14]. Che-Wei Chou ,Chih-Sheng Hou and Jin-Fu Li "Built-in self-diagnosis and test time reduction techniques for NAND flash memories" International Symposium on VLSI Design, Automation and Test (VLSI-DAT),April 2011.

[15]. Jen-Chieh Yeh, Kuo-Liang Cheng, Cheng-Wen Wu and Yung-Fa Chou, "Flash Memory Testing and Built-In Self-Diagnosis with March-Like Test Algorithms", IEEE Transactions on Computer-Aided Design Of Integrated Circuits and Systems, Vol. 26, No. 6, pp: 1101-1113, JUNE 2007.

[16]. Masnita, Wan Zuha W.H, R.M. Sidek and A. Halin, "The data and read/write controller for March-based SRAM diagnostic algorithm MBIST", proceedings of 2009 IEEE conference on Research and Development, Nov.2009.

[17]. Manikandan.B and Praveen kumar.J, "A VLSI Implementation of High Speed FSM-based programmable Memory BIST Controller", Journal of Electronics and Communication Engineering Research, Vol.1, No.2, pp: 01-06, 2013.

[18]. K.Padma Priya, "High Speed FSM-based programmable Memory Built-In Self-Test (MBIST) Controller", International Journal of Computer Science and Mobile Computing, Vol. 2, No. 2, pp:.46-52, February 2013.

[19]. M. Jahnavi, P. S. Indrani, M. J. C. Prasad, "Implementation of Concurrent Online MBIST for RFID Memories using March SS Algorithm", International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol.3, No.6, November 2013.