Optimized ALU with BIST Implementation Using Cadence Encounter Platform

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***Abstract*—*The* aim of this project is to optimize an Arithmetic Logical Unit with BIST capability. Arithmetic Logical Unit is used in many processing and computing devices, due to rapid development of technology the faster arithmetic and logical unit which consume less power and area required.Due to the increasing integration complexities of IC's the Optimized Arithmetic Logical Unit implement sometimes may mal-function, so testing capability must be provide and this is accomplished by Built-In-Self-Test (BIST).So this project has been done with the help of Verilog Hardware Description Language, Simulated by Xilinx10.1 Software and is synthesized by cadence tool. After synthesis Area and power are reduced by 31% and 42% respectively.**

***Keywords*—Optimized ALU, Ripple Carry Adder, Vedic Multiplier, Built-In-Self-Test.**

I. INTRODUCTION

Arithmetic Logic Unit (ALU) is an important and necessary unit present in every processors and all computing devices performing arithmetic operations like addition, subtraction, multiplication, increment, decrement, shifting and logical operations like and, or, not, XOR. The ALU must be optimized and when manufactured they might have defects or might be faulty hence to increase testability, Design For Testability(DFT) must be provided one such methodology is Built-In-Self-Test (BIST). BIST technique provides little cost, a well-defined increase in the testability of the Circuit under Test (CUT). The test pattern generator is a part of BIST implemented using linear feedback Shift Register (LFSR), this increases the testability of ALU.

II. EXISTING SYSTEM

The multiplication dominates the execution time of most DSP algorithms; so there is a need of high speed multiplier.The array multipliers used in the existing ALU involves more number of multiplication steps and hence the complexity is increased which in turn increases delay and area. So the power consumption is more.

III. PROPOSED SYSTEM

This system is proposed for high speed, low power consumption, less delay and reduced area. Fast adders like Ripple Carry Adders are used for addition and Fast multipliers which involves Vedic Multiplier technique is used for multiplication that reduces area, delay and power consumption. Hence the Optimization of ALU is achieved.

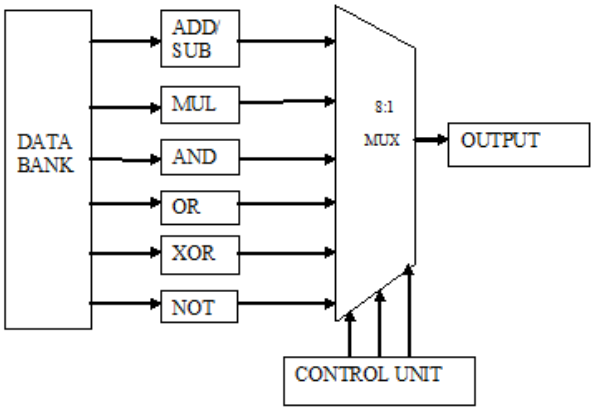

Figure 1: Block diagram of proposed Arithmetic Logical Unit

After the design and implementation of optimized ALU, BIST has to be implemented to increase the testability of the ALU. The BIST consists test pattern generators like LFSR(Linear Feedback Shift Register) which generates test patterns and these test patterns are applied to circuit under test, that is optimized ALU and then obtained result can be analyzed and checked for the correctness of ALU.

The Ripple Carry Adder reduces the propagation delay during addition when the partial products are added. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder.

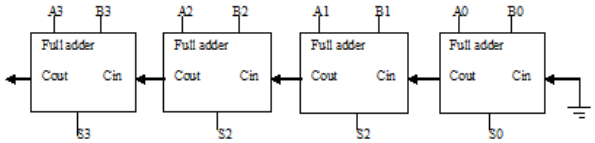

Figure 2: Block diagram of Ripple Carry Adder

Multiplier unit is optimized using Vedic Multiplier technique called as Urdhva Triyagbhyam sutra. This increases speed of multiplier.

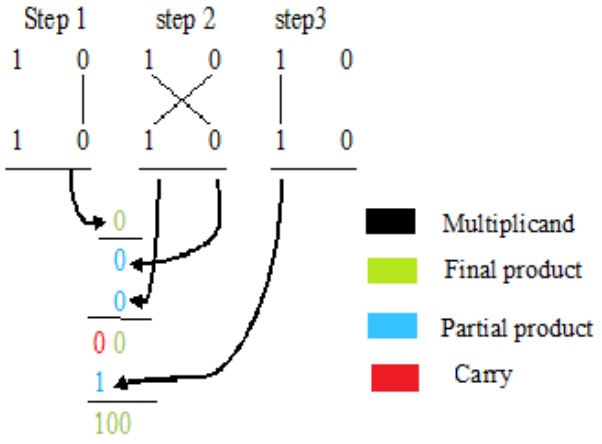

Figure 3: 2x2 Vedic Multiplication

Here the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to gives the bit and the carry. The carry becomes the fourth bit of the final product.

Consider two 4-bit binary numbers a3a2a1a0 and b3b2b1 b0. The partial products (P7P6P5P4P3P2P1P0) generated are given by the following equations:

i. P0= a0b0
ii. P1= a0b1 + a1b0
iii. P2 = a0b2 + a1b1 + a2b0+ P1
iv. P3= a0b3 + a1b2 + a2b1 + a3b0+ P2
v. P4 = a1b3 + a2b2 + a3b1 + P3
vi. P5 = a1b2 + a2b1 + P4
vii. P6 = a3b3 + P5
viii. P7 = carry of P6

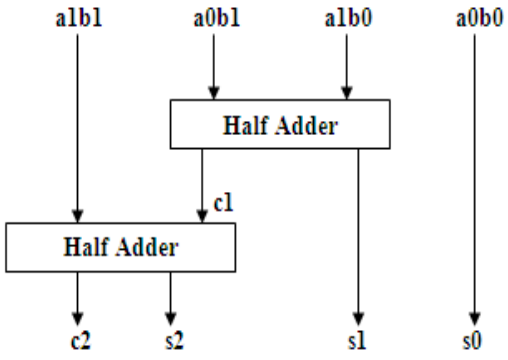

Figure 4: Block diagram of 2x2 Vedic multiplier

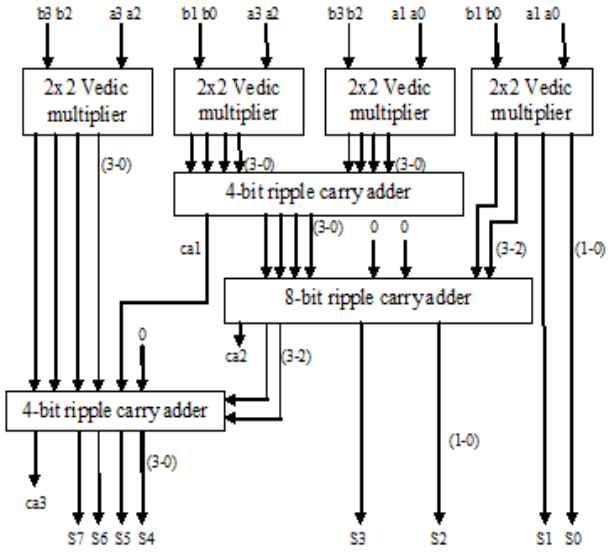

Figure 5: Block diagram of 4x4 Vedic multiplier

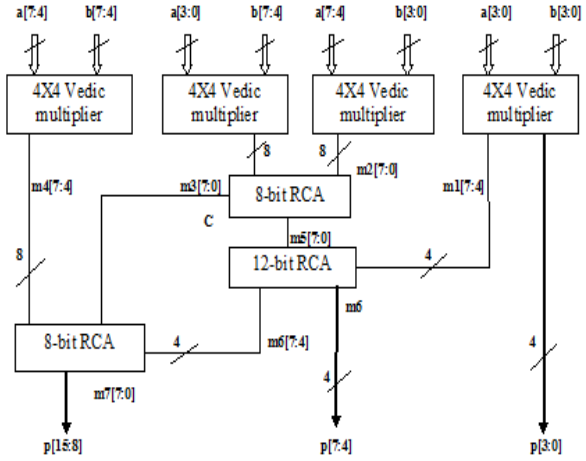

Figure 6: Block diagram of 8x8 vedic multiplier

IV. BIST IMPLEMENTATION

Built-In-Self-Test is a design technique in which parts of circuits are used to test the circuit itself. Parts of a circuit that must be operational is used to execute a self-test. The figure 3 shows typical BIST hardware. After designing and implementing Optimized ALU, BIST has to be implemented, it has BIST controller which selects whether it should work either in testing mode or normal mode. It has test pattern generators like LFSR linear feedback shift register which generates test patterns these test patterns are applied to circuit under test that is optimized ALU over here then the result obtained is analyzed and checked for correctness of ALU. comparator compares the signature produced by the data compactor with a reference signature stored in a ROM. If both the responses are matched then the circuit is good, otherwise it is faulty.

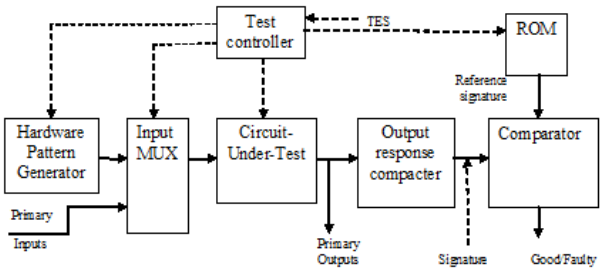

Figure 7: BIST Process

The components included in the BIST Process are ROM, Circuit under test (CUT), 8:1 Mux, Comparator, D flip-flop, Test pattern generators like Linear feedback shift register (LFSR).

ROM: Read-only memory (usually known by its acronym, ROM) is a class of storage media used in computers and other electronic devices. The data stored in ROM cannot be modified.

Circuit-under-test: CUT is the term used to refer to a circuit undergoing testing, either at first manufacture or later during its life cycle as a part of on-going functional testing and calibration checks.

Linear Feedback Shift Register: This is hardware that generates an exhaustive or pseudo-random pattern sequence of test patterns, and can also be used as a response compacter.

8:1 Mux: A multiplexer is a device that selects one of several input signals and forwards the selected input into a single line. A multiplexer is also called as a data selector. This provides full binary decoding to select one of eight input data sources.

Comparator: Comparator is used to compare two binary numbers.

V. RESULTS

The output waveforms of BIST is obtained as shown in figure 8 and the RTL schematic of the ALU and BIST are shown in figure 9 and 10 respectively. The synthesis results are shown in table 1and 2. After encounter the power and areaare reduced by 31% and 42% respectively.

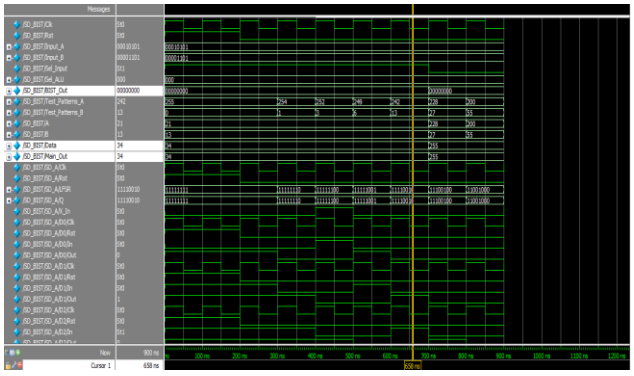

Figure 8:BIST output waveforms

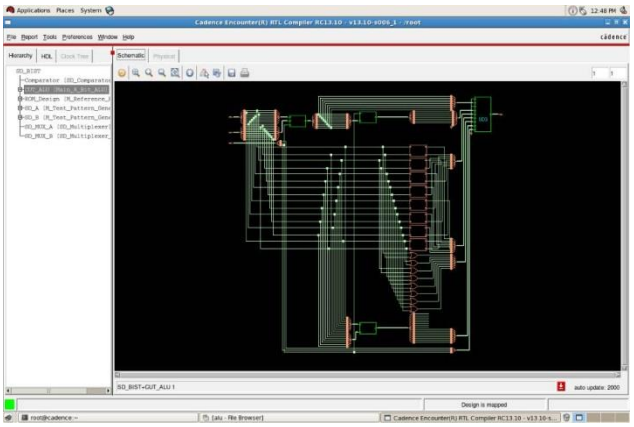

Figure 9: RTL schematic of ALU

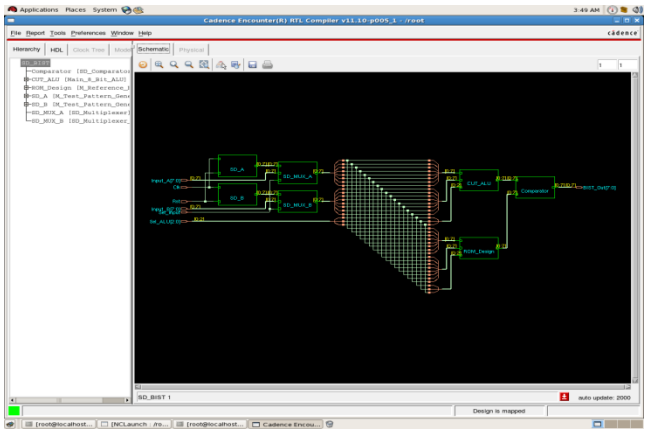

Figure 10: RTL Schematic of BIST.

Table1: Power consumed by various instances after encounter.

Instances	Cells	Leakage Power(nw)	Dynamic Power(nw)	Total Power(nw)
SD_A	19	406.847	2105.239	2572.086
SD_B	27	444.381	2288.771	2733.152
SD_MUX_A	9	117.632	2732.819	2850.451
SD_MUX_B	9	124.876	2509.528	2634.404
CUT_ALU	211	5046.686	37083.439	42130.125
ROM_Design	229	3166.953	23985.210	27152.164
Comparator	8	166.879	322.028	488.907
SD_BIST	512	9472.254	72136.565	81610.819

Table 2: Area occupied by various instances after encounter

Instance	Cells	Cell Area(μm^2)	Net Area(μm^2)	Total Area(μm^2)
SD_A	19	152	0	152
SD_B	27	169	0	169
SD_MUX_A	9	47	0	47
SD_MUX_B	9	47	0	47
CUT_ALU	211	1439	0	1439

ROM_Design	229	1087	0	1087
Comparator	8	45	0	45
SD_BIST	572	2988	0	2988

VI. CONCLUSION

In this project we are implementing Optimized ALU with BIST capability which has lesser area, power and delay using Carry save adder and Vedic multiplier with testing capability provided by Built-in-Self-Test.

A. Future Scope

This project can also be carried out using two architectures FPGA and ASIC. By providing timing constraint and gate level implementation we can further optimize the power and area.

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