Design Specification for CMOS Camera Configuration

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***Abstract*- The scientific cameras play a major role in the accomplishment of instrument and mission goals. In consequence, every camera requirement shall harmonize with both mission and instrument. This paper defines the camera electronics functionality, describing its architectural design, and addresses the fulfillment of its performance requirements.**

***Keywords*- Functional Description, Physical design, Physical Verification, Post Layout, Design Rules.**

I. INTRODUCTION

This paper introduces the development of a CMOS (Complementary Metal Oxide Semiconductor) Camera Configuration for ASIC (application specific integrated circuit). This ASIC is the part of "Miniature Camera System", based on a commercial off-the-shelf (COTS) camera module. The COTS Camera module consists of optics, sensors and has versatile features such as HD resolution, integrated digitizer, signal processing electronics, inbuilt JPEG compression etc. This camera requires clock as control signal and I^2C bus signals for its configuration in addition to supply for its operation. The camera outputs 8-bit parallel data along with frame and line sync signals and a pixel clock. Therefore it requires a host module which can cater to provide configuration bits to control the camera and also take output from it for further processing.

II. FUNCTIONAL DESCRIPTION

Camera Configuration ASIC consists of Reset, CLK and Mode Selection signals as input. Reset signal marks the beginning of all operations. CLK signals is used for ASIC internal operation and to generate various signals (CLK_B, SDA, and SCL) for Camera Module. There are 16 different modes proposed for camera to function therefore 4 mode selection bits are to be provided by user-interface. These mode selection bits will be used by ASIC to configure the camera through I^2C [1] interface (SDA, SCL signals) to decide the kind of output that will be obtained from camera viz. uncompressed or compressed images with desired frame rates. The configuration parameters for camera module are stored in pre-fixed ROM within ASIC. The camera module communicates via a 2-wire I^2C [2] interface with the host (ASIC) and thus SCL (serial clock) and SDA (serial data) signals are required for configuration of the camera module. This is a half-duplex communication in which SDA is Bi-Directional while SCL is unidirectional. Also camera provides 8 bit parallel data along with horizontal and vertical sync signals (HSYNC, VSYNC) and a pixel clock (PCLK). All these signal are required to be sent to user-interface via ASIC and therefore ASIC must act as a buffer for these signals.

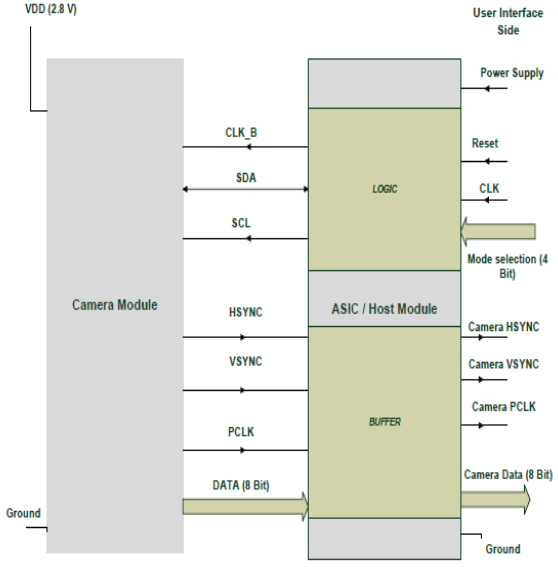

Fig: Block diagram of CMOS camera configuration ASIC

III. PHYSICAL DESIGN

A) FLOORPLANNING

In floorplanning we estimate sizes and set the initial relative locations of the various blocks in our ASIC. At the same time we allocate space for clock and power wiring and decide on the location of the I/O and power pads.[3] The input to a floorplanning tool is a hierarchical net list that describes the interconnection of the blocks (RAM, ROM, ALU, cache controller, and so on); the logic cells (NAND, NOR, D flip-flop and so on) within the blocks; and the logic cell connectors (the terms terminals, pins, or ports mean the same thing as connectors). The net list is a logical description of the ASIC; the floorplan is a physical description of an ASIC. Floorplanning is thus a mapping between the logical

description (the net list) and the physical description (the floorplan).

The goals of floorplanning are:

- Arrange the blocks on a chip.
- Decide the location of the I/O pads.
- Decide the location and number of the power pads.
- Decide the type of power distribution.

The objectives of floorplanning is to minimize the chip area and minimize delay.

B) POWER PAD CALCULATION

Power pads [4] are placed according to predefined Library guidelines as follows:

Maximum distance to Power PAD (PVDI, PV0I, PVDC, PV0C) in I/O no. in 4LM Process allowed for ESD is

Maximum distance in I/O no. =

$$\frac{\text{Maximum resistance allowed}}{\text{Metal Resistivity} * (\text{IO pitch}/\text{Metal width})}$$

Here Maximum resistance allowed for ESD = 2 Ohm
Metal Resistivity = 56 mOhm/sq
Metal Width = 30 μm(VSS Rail Width for top metal in PV0I)

C) PLACEMENT

Placement defines the location of the logic cells within the flexible blocks and sets aside space for the interconnect to each logic cell. Placement for a gate array or standard – cell design assigns each logic cell to a position in a row. Placer tool chooses which of the fixed logic resources on the chip are used for which logic cells.

D) CLOCK TREE SYNTHESIS

Ideally the clock signal will arrive to all flip-flops at the same time. Due to variations in buffering, loading, and interconnect lengths, the clock's arrival is skewed. A clock-tree insertion tool evaluates the loading and positioning of all clock related signals and places clock buffers in the appropriate spots to minimize skew to acceptable levels.

E) ROUTING

Once the designer has floor-planned a chip and the logic cells within the flexible blocks have been placed, it is time to make the connections by routing the chip. Routing makes the connections between logic cells. Routing is usually split into global routing followed by detailed routing. Global routing determines where the interconnections between the placed logic cells and blocks will be situated. Only routes to be used by the interconnections are decided in this step, not the actual locations of the interconnections within the wiring areas. Global routing is sometimes called loose routing for this reason, Local routing joins the logic cells with interconnections. Information on which interconnection areas to use comes from the global router. Only at this stage of layout do we finally decide on the width, mask layer, and exact location of the interconnections. Local routing is also known as detailed routing.

F) METAL FILL

Metal fill insertion improves surface planarity for each metal layer by inserting metal fill segments to meet specified density requirements, Improved surface planarity helps to decrease manufacturing variations that contribute to timing variability. This, in turn, helps to increase yield numbers. So Dummy fill insertion has been done in Virtuoso Layout Editor and Calibre to take care of minimum and maximum metal density rule

IV . FORMAL VERIFICATION (POST LAYOUT)

Formal verification utilizes mathematical techniques to compare the logic to be verified against either a logical specification or a reference design. Unlike verification through simulation, formal verification does not require input vectors. As formal verification considers only logical functions during comparisons, it is independent of the design's physical properties, such as layout and timing.

IV. PHYSICAL VERIFICATION

A) DESIGN RULE CHECK

Layout rules also referred to as design rules, can be considered as a prescription for preparing the photo masks used in the fabrication of IC's. The rules provide a necessary communication link between circuit designer and process engineer during the manufacturing phase. The main objective associated with layout rules is to obtain a circuit with optimum yield in as much as small an area as possible without compromising reliability of the circuit. In general, design rules represent the best compromise between performance and yield.

Design rules specify the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs. The rules represent a tolerance that that ensures very high probability of correct fabrication and subsequent operation. Any significant or frequent departure form design rules will seriously prejudice the success of a design Two sets of design rule constraints in a process relate to line widths and interlayer registration. If the line widths are made too small, it is possible for the line to become discontinuous, thus leading to an open circuit wire. On the other hand, if the wires are placed too close to one another it is possible for them to merge together; i.e. Shorts can appear between two independent circuit nets. Furthermore the spacing between

two independent layers may be affected by vertical topology of the process

B) DESIGN RULE CHECK FOR ANTENNA

In chip manufacturing, gate oxide can be easily damaged by electrostatic discharge.[5] The static charge that is collected on wires during the multilevel metallization process can damage the device or lead to a total chip failure. The phenomena of an electrostatic charge being discharged into the device are referred to as either antenna or charge-collecting antenna problems. Antenna fixing is performed on long wires to reduce charge accumulation during manufacturing. To prevent antenna problems, IC Compiler verifies that for each input pin the metal antenna area divided by the gate area is less than the maximum antenna ratio given by the foundry:

(antenna-area)/(gate-area) < (max-antenna-ratio)

The antenna flow consists of the following steps:

1. Define the antenna rules.
2. Specify the antenna properties of the pins and ports.
3. Analyse and fix the antenna violations.

Antenna rules defined in IC compiler and Calibre DRC runset file are different. So manual modification in routing has been done in Virtuso Layout Editor by jumper insertion to take care
of Antenna rules.

V. CONCLUSION

This paper has tackled the definition, design, development, and qualification of new camera electronics with the purpose of optimizing them for application specific integrated circuit. Upcoming generations of CMOS camera will propel towards integrating various categories of snapshots and shutter features with high tolerances against radiation, thus providing future observatories with superior temporal resolution and standard quality.

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