A Comparative Study of Power Dissipation of Sequential Circuits for 2N-2N2P, ECRL and PFAL Adiabatic Logic Families

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***Abstract*— Recent advances in compact, practical adiabatic computing circuits which demonstrate significant energy savings have renewed interest in using such techniques in low-power systems. In this paper power consumption of different sequential circuits like brute force latch , master slave D-flip flop and parallel-in-parallel-out shift registers based on different adiabatic logic families like 2N-2N2P, ECRL, PFAL were compared at 180 nm technology . Power consumption of PFAL adiabatic logic family is least in comparative to 2N-2N2P and ECRL adiabatic logic families. Maximum power consumption is obtained in ECRL family i.e. approximately 2.5 times greater than power consumption of 2N-2N2P logic family and 3.5 times greater than power consumption of PFAL logic family at various frequencies ranging from 350MHz to 500MHz.**

***Keywords*- adiabatic logic design,master slave flip flop,low power sequential circuit,VLSI,shift registers.**

I. INTRODUCTION

A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances, which cause power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. In the literature, a multitude of adiabatic logic families are [1]-[11] .Each different implementation shows some particular advantages, but there are also some basic drawbacks for these circuits. The goal of this paper is to compare different adiabatic logic families by investigation of power dissipation and delays of some basic sequential circuits. For this purpose three adiabatic logic families 2N-2N2P, ECRL and PFAL are evaluated. The proposed circuits have been simulated and demonstrate adiabatic power savings over an operating frequency range from 350MHz to 500MHz at 180 nm technology.

A. Adiabatic switching

Adiabatic switching operation is an ideal condition, which may only be approached asymptotically as the switching process is slowed down. For adiabatic operation in circuit we assume that load capacitance is charged by constant current source not by constant voltage source as done in conventional digital CMOS circuits.

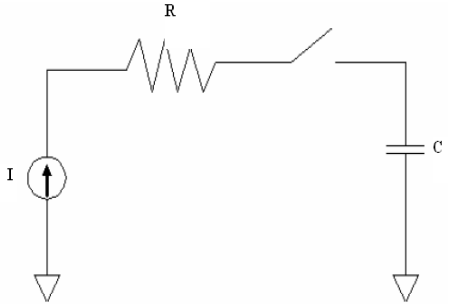

Fig. 1 Circuit explaining adiabatic switching

In adiabatic operation constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage V_c is zero initially, the variation of the voltage as a function of time can be found as:

$$V_c(t) = \frac{1}{c} \, . I_{source} \, . t$$

The amount of energy dissipated in the resistor R from $t = 0 \; to \; t = T$ can be found as:

$$E_{diss} = R \int_0^T I_{source}^2 \, dt = R . I_{source}^2 \, . T$$

So we can also express the dissipated energy during this charge-up transition as follows:

$$E_{diss} = \frac{RC}{T} C V_c^2(T)$$

From above equation we can see that if charging time T is larger than 2RC, the dissipated energy can be made small. Adiabatic logic circuit requires non standard power supplies with time varying voltage, called pulsed power supply.

B. Phases in an Adiabatic Power Supply:

The constant current source needed for the adiabatic operation is usually a trapezoidal or sinusoidal voltage source. In an adiabatic circuit, the power supply also acts as a clock. Hence it is given the term power clock.

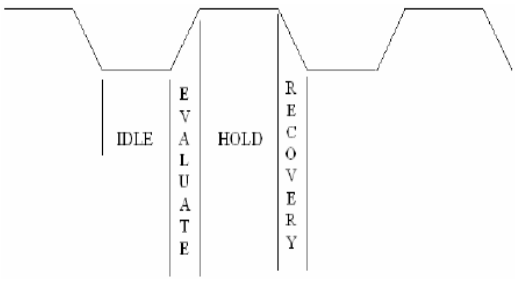

Fig.2 Phases in an Adiabatic Power Supply

In above figure 2 the trapezoidal waveform is shown with its four phases. Initially the adiabatic supply is in the ideal/wait phase and supply voltage is low, maintained at the same time ,the output in the low state. Then inputs are set and supply ramps up. As the inputs are evaluated the outputs change complimentary to each other and the one that goes high follows the power supply until it reaches V_{dd}. At the moment the inputs are returned to the low state and after the certain period of time in the HOLD "1 " phase, the supply ramps down with the outputs following until the LOW state is reached again. That is to say, during the idle /wait phase, the circuit idles. In the EVALUTE phase, the load capacitance either charges up or does not depending upon the inputs to functional blocks. In the HOLD phase the output is kept at steady, so that subsequent stage can evaluate. Finally in the recovery or RESET phase, the charge held on capacitance is recovered. Practical adiabatic circuits use sinusoidal clock with the duration of the HOLD phase tending to zero.

C. Adiabatic Logic Families:

Out of the many adiabatic logic families proposed in the literature three are chosen: the Efficient Charge Recovery Logic (ECRL) [7] , the Positive Feedback Adiabatic Logic (PFAL) [10], [11] and the 2N-2N2P [2].

1.) *Efficient Charge Recovery Logic:* This logic is shown in Figure 3, uses two crossed coupled PMOS transistors **m1** and **m2** and two NMOS transistors in the N-functional blocks. An AC power supply **pwr** is used for ECRL gates, so as to recover and reuse the supplied energy. Both **out** and **/out** are generated, so that power clock generator can always drive the constant load capacitance, independent of the input signal. Full output swing is obtained because of the cross coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of PMOS transistors, the circuits suffer nonadiabatic loss both in precharge and recover phases. That is ECRL always pumps charge on the output with the full swing. However as the voltage on the supply clock approaches to the $|V_{tp}|$, the PMOS transistors gets turned off.

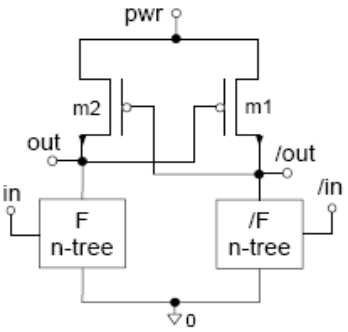

Fig.3 Basic structure of ECRL logic

So the recovery path to the supply clock is disconnected, thus, resulting in incomplete recovery -$|V_{tp}|$ is the threshold voltage of PMOS transistors. The amount of loss is given as

$$E_{ECRL} = \frac{1}{2} C V_{|TP|}^2$$

The ECRL circuits are operated in a pipelining style with the four phase supply clocks. When the output is directly connected to the input of next stage (which is the combinational logic), only one phase is enough for the logic value to propagate. The major disadvantage of this circuit is the existence of coupling effect. Because the two outputs are connected by the PMOS latch and the two complimentary outputs can interfere each other.

2.) *2N-2N2P Adiabatic Logic:* This was proposed as a modification of ECRL logic, in order to reduce the coupling effect. General schematic of 2N-2N2P logic is given below:

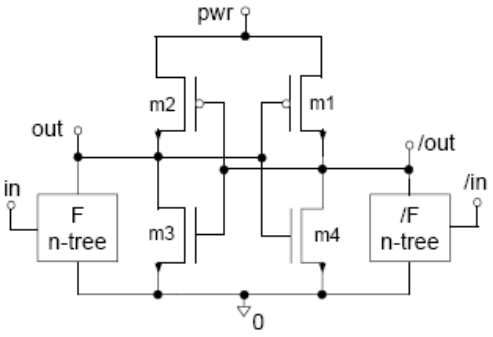

Fig. 4 Basic structure of 2N-2N2P logic

The 2N-2N2P logic uses the cross coupled latch of two PMOS and two NMOS (**m1-m4**), as in Figure 4, instead of only two NMOS as shown in ECRL logic family. The N- functional block is in parallel with NMOS of latch and thus occupies additional area, but the primary advantage of 2N-2N2P over ECRL is that the cross coupled NMOS switches results in non floating output for large part of recovery phase. The 2N-2N2P uses two cross coupled PMOS transistor for both precharge and recovery, thus its energy loss per cycle is given by the following expression:

$$E_{2N-2N2P} = \left(2\frac{R_P C_L}{T}\right) C_L V_{dd}^2 + C_L V_{TP}^2$$

In above equation the first term represents the full adiabatic loss, which can be reduced by lowering the operation frequency, and the second term represents the non-adiabatic loss in energy, which is independent of operation frequency.

3.) *Positive Feedback Adiabatic Logic (PFAL):* The partial energy recovery structured named positive feedback adiabatic logic has been used, since it shows the lowest energy consumption if compared to another similar family and good robustness against technological parameter variations. It is a dual rail circuit with partial energy recovery. The general schematic of PFAL structure is shown in Figure 6. The core of PFAL is made with the adiabatic amplifier, a latch made by the two PMOS **m1-m2** and by the two NMOS **m3-m4**, that avoids the logic level degradation on the output nodes **out** and **/out**. The two n-trees realize the logic functions this logic family also generates both positive and negative output. The functional blocks are in parallel with the PMOSFETS of adiabatic amplifier and form the transmission gates. The two n-trees realize the logic functions.

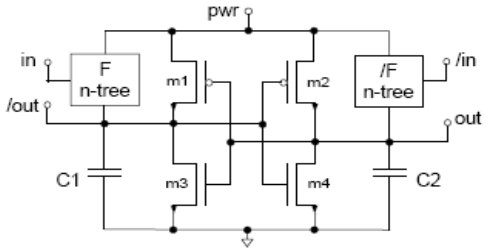

Fig. 5 Basic structure of PFAL logic

The circuit to the power clock generator; the HOLD PHASE and IDEAL PHASE are needed for The two major differences with respect to ECRL are that the latch is made by two PMOS and two NMOS, rather than by only two PMOS, as in the ECRL logic, and that the functional blocks are in parallel with the transmission PMOS. Thus the equivalent resistance is smaller when the capacitance needs to be charged. It uses the four phase power clock as shown in Figure 2, *pwr(t)* rises from 0 to V_{dd} in the EVALUTE phase and supplies energy to the circuit, then *pwr(t)* returns to 0 in the RECOVERY PHASE and the energy flows back from cascading gates.

B Sequential Circuits

1.) *Brute Force D-Latches:* In this section brute force D latches are presented with applying adiabatic logic technique under three considered families 2N-2N2P, ECRL and PFAL. The latches are characterized for power consumptions and propagation delay using 180nm with using 3.3V sine wave power supply. The latch considered in this section consists of a cross-coupled inverter pair, a driver inverter, and a transmission gate controlled by the clock signal as shown in Fig 7.

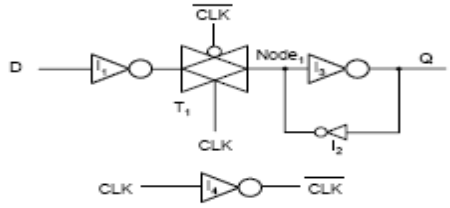

Fig.6 Basic structure of Brute Data force D- Latch

The advantages of this latch are the reduced clock load and the lower transistor count as compared to a latch that can disable the feedback path whenever the latch is transparent. To be able to transfer new data into this latch, the driver inverter (I_1) and the transmission gate (T_1) must be stronger as compared to the feedback inverter (I_2) . Above circuit is made for each considered three adiabatic logic families seperatly. Simulation result for above circuit is shown below:

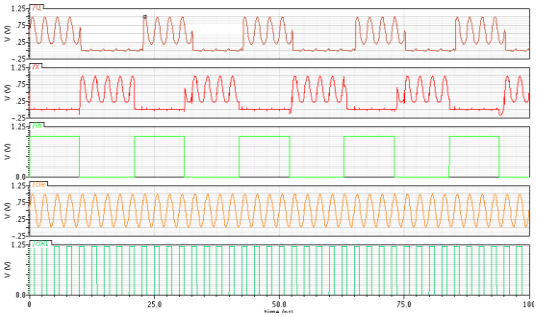

Fig. 7 Simulation results of Data forcing D-Latch

The influence of different adiabatic logic family on power dissipation is investigated by means of CADENCE software at 180nm technology. In order to determine the energy dependence on three adiabatic logic families and on the frequency the three brute force D latches are simulated for the whole useful frequency range. Figure 9 shows the power consumption per switching operation of D-latches for the three logic families.

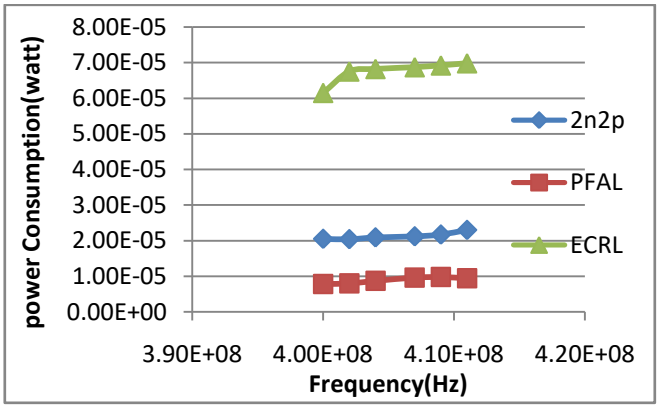

Fig. 8 Frequency Vs Power consumption of D-Latches of 2N-2N2P, ECRL and PFAL adiabatic logic families

The supply voltage is 3.3 V. For high frequencies the behavior is no more adiabatic and therefore the energy consumption increases. At low frequencies the dissipated energy increases for adiabatic gates due to the leakage currents of the transistors. Thus for each employed logic family an optimal interval for the operating frequency is obtained, that we call "Adiabatic frequency range". This adiabatic frequency range for brute force D latches for three families is 400 to 410 MHz.

2.) *Master-slave flip-flop:* The circuits considered in this section are master-slave flip-flop based on the brute-force latch architecture shown in Figure 7. The gate level schematic of the brute-force flip-flop is shown in figure 10, to be able to transfer new data to the master stage when the clock signal is high, I_1 and T_1 must be significantly stronger than I_2. Similarly, to be able to change the state of the slave stage when the clock is low, I_3 and T_2 must be significantly stronger than I_5.

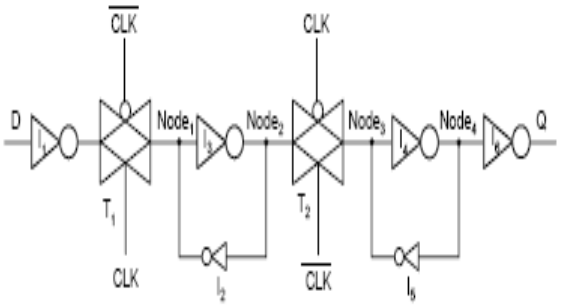

Fig. 9 Basic structure of Master Slave D-FF

Simulation results for comparison of power consumption for master slave flip flop based on three adiabatic logic families is shown in figure 11. The optimal interval for the operating frequency for master slave D-ff is 420MHz to 470 MHz.

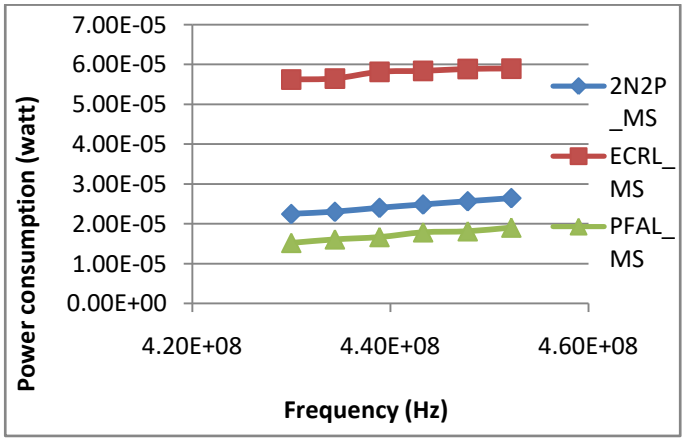

Fig. 10 Adiabatic frequency range for Master Slave flip flop is 430 to 455 MHz.

3.) *Parallel-In-Parallel-Out Shift Register:*

The circuits considered in this section are Parallel-In-Parallel-Out shift register is made of Master-Slave D- flip flop shown in figure 10.

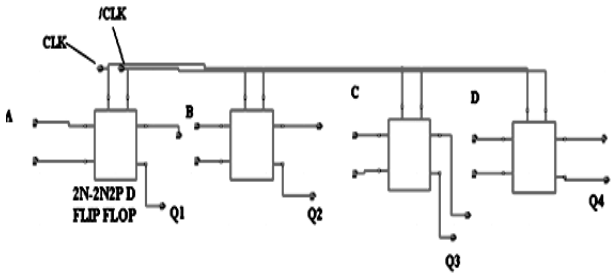

Fig. 11 Basic structure of Parallel-In-Parallel-out shift register

The register shown in above figure 12, each flip flop is made of 2N-2N2P logic technique. By this same way we have designed the registers for other logic techniques ECRL and PFAL, simply by replacing the each flip flop with corresponding logic technique flip flop. Simulation results for comparison of power consumption for Parallel-In-Parallel-Out Shift Register: based on three adiabatic logic families is shown in figure 13. The optimal interval for the operating frequency for Parallel-In-Parallel-Out shift register is 490MHz to 510 MHz

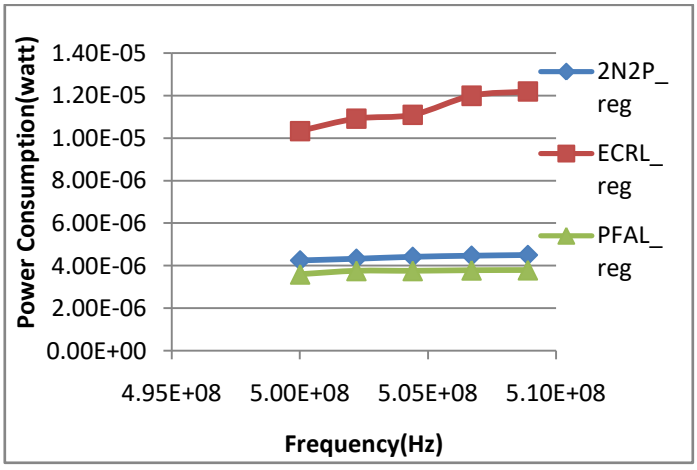

Fig. 12 Frequency Vs Power consumption of Parallel-In-Parallel-Out Shift Registers of 2N-2N2P, ECRL and PFAL adiabatic logic families

II. CONCLUSIONS

In this work I discussed three approaches 2N-2N2P, ECRL and PFAL for design of low power digital circuits. I have implemented sequential circuits example Flip flops (D-Flip Flop), Latches (D-Latch), Register (Parallel-In-Parallel-Out Shift Register) using above three adiabatic logic families. All components of digital circuits are designed from cadence tool, using gpdk 0.90 and gpdk 0.18 µ m technology with 1.0 V and 3.3V power supply. Power consumptions of different families are compared for D-Latches, Master slave D-Flip Flops and for Registers. In which, we can see that PFAL logic family gives best results in comparisons of remaining two. Delays of outputs with respect to inputs and power clock are also shown at particular frequency as follows:

Table I. Comparisons of delays of Data forcing D-Latches of different adiabatic Logic families at 411MHz frequency

	ECRL Data Force D-Latch	2N2N-2p Data Force D-Latch	PFAL Data Force D-Latch
$T_{D\rightarrow Q}(0\rightarrow1)$	1.80ns	2.02ns	2.67ns
$T_{D\rightarrow Q}(1\rightarrow0)$	0.73ns	1.87ns	2.46ns
Delay of output with respect to clock	3.01ns	2.20ns	0.83ns

Table II. Comparisons of delays of Master Slave D-Flip Flops of different adiabatic Logic families at 452MHz frequency

	ECRL Master Slave D-Flip Flop	2N2N-2p Master Slave D-Flip Flop	PFAL Master Slave D-Flip Flop
$T_{D\rightarrow Q}(0\rightarrow1)$	2.99ns	1.46ns	4.02ns
$T_{D\rightarrow Q}(1\rightarrow0)$	1.29ns	1.38ns	2.79ns
Delay of output with respect to clock	1.49ns	1.86ns	0.413ns

Table III. Comparisons of delays of Parallel-In-Parallel-Out shift register of different adiabatic Logic families at 450 MHz frequency

	ECRL Parallel-In-Parallel-Out shift register	2N2N-2PParallel-In-Parallel-Out shift register	PFAL Parallel-In-Parallel-Out shift register
$T_{D\rightarrow Q}(0\rightarrow1)$	1.80ns	2.02ns	2.67ns
$T_{D\rightarrow Q}(1\rightarrow0)$	0.73ns	1.87ns	2.46ns

We can see that delay for PFAL is maximum , and for ECRL, it is minimum. But sometimes we get minimum delay in 2N-2N2P logic family, i.e. sometimes delay in ECRL logic family is greater then 2N-2N2P logic family.

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