Dynamic Power Reduction in Linear Feedback Shift Register Using Look Ahead Clock Gating Technique

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***Abstract*—In this paper, a novel Linear Feedback Shift Register (LFSR) with Look Ahead Clock Gating (LACG) technique is presented to reduce the power consumption in sequential circuits. Clock gating is a predominant technique used to reduce unwanted switching of clock signals. Several clock gating techniques to reduce the dynamic power have been developed, of which LACG is predominant. LACG computes the clock enabling signals of each flip-flop (FF) one cycle ahead of time, based on the present cycle data of the flip-flops on which it depends. It overcomes the hardware overhead and timing problems in the existing clock gating methods like data-driven clock gating and Auto-Gated flip-flops (AGFF) by allotting a full clock cycle for the determination of the clock enabling signals. Simulation results shows that the LFSR with the Look-Ahead Clock Gating technique achieves power savings on an average of 81.44% compared to the conventional LFSR and data-driven clock gating LFSR.**

Keywords—LACG; LFSR; AGFF; data-driven; timing problems

I. INTRODUCTION

The sequential circuits in a system are considered major contributors to the dynamic power consumption since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, which is responsible for 30% - 70% of the total dynamic power consumption [1]. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal, regardless of whether or not they will toggle in the next cycle. With clock gating, the clock signals ANDed with explicitly predefined enable signals [2][3]. Clock gating is employed at all levels like system architecture, block design, logic design, and gates [4].

LFSR is a sequential circuit commonly used in Built In Self Test (BIST), Signature analysis and in Spread spectrum communications. In the applications like pseudo-random bit generators (PRBGs), linear feedback shift register is used to produce a random sequence. A good PRBG must be characterized by repeatability (i.e. giving the same output sequence when the same seed is used) and randomness (i.e., passing the most common standard tests and giving good statistical properties) [5]. Today, hardware implementation of the PRBGs is almost always made up of the well-known linear-feedback shift register whose generic circuit is reported in the Figure. This circuit is very simple to be implemented, but since the clock-path of all flip-flops (FFs) toggle at every clock cycle, they consume a significant amount of power. This problem was extensively addressed in [lowy96]. The scheme based on gated clock design for LFSR is proposed in [5]. This design achieves better power result but due to hardware overhead involved this may not work for large applications.

Different clock gating techniques have been used to minimize the clock power consumption, as it is the main source of chip power consumption. Deactivating the clock signal leads to reduced power consumptions of both its internal nodes and clock lines, but the overhead involved limits its use in low data switching situations. The main purpose of this project is to reduce the clock gated flip-flop overhead and make it applicable to data signals with higher switching activity.

II. LINEAR FEEDBACK SHIFT REGISTER

LFSR is a well-known circuit for pseudo-random number generation, which consists of N registers connected together as a shift register. The input to the LFSR comes from the XOR of particular bits of the register. On reset, the registers must be initialized to a non-zero value (eg. all 1's). At each clock tick, the feedback function is evaluated using the input from tapped bits. The result is shifted into the leftmost bit of the register and the rightmost bit is shifted into the output [6].

The LFSR is an example of maximal length shift register because its output sequences through all 2^N-1 combinations (excluding all 0's) which is shown in the Fig. 1. The inputs fed to the XOR are called the tap sequence and are often specified with a characteristic polynomial. For example, 4 – bit LFSR has characteristic polynomial $1+x^3+x^4$ because the taps come after the 3rd and 4th registers.

III. COMMON CLOCK GATING METHODS

When the FF input is not toggling, then effectively

shutting off the clock to that FF for particular instant of time and reduce dynamic power consumption. Clock gating is very useful for reducing the power consumed by the sequential circuits. Some commonly used clock gating techniques are described below,

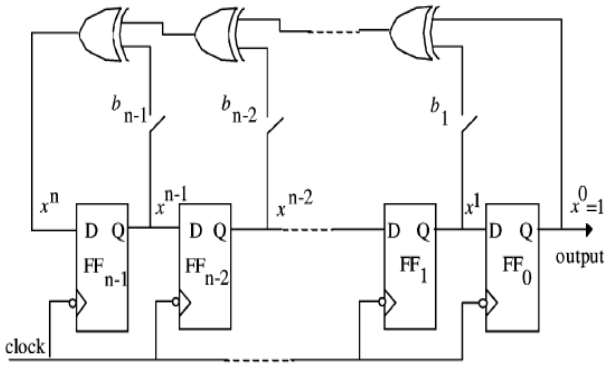

Fig. 1 Schematic of N-bit traditional LFSR

A. Synthesis based clock gating

Gated positive latch is shown in the Fig. 2. The comparison between input D and output Q is done by an XOR gate which feeds the AND gate to produce the required gated clock signal (Clkg) for the latch. When both D and Q are the same, the gated clock signal will remain low and will not consume power for switching [7]. When they differ, the gated clock signal will copy the original clock and may make a necessary transition to change the state of the latch. The same technique can be used for gated negative latch by using XNOR gate and OR gate.

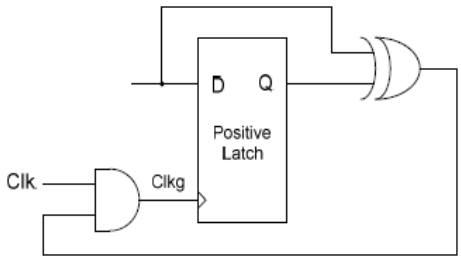

Fig. 2 Clock gated positive latch

Advantages

The gated flip-flop is implemented by cascading two clock-gated latches in a master-slave configuration and this design overcomes the timing constraints.

Disadvantages

The design needs two gating overhead circuits for each flip-flop. This double overhead limits the use of flip-flop on data signals with low switching activity.

B. Data driven clock gating

A Flip-Flop finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The data-driven clock gating is shown in the Fig. 3. The outputs of *k* XOR gates are ORed to generate a joint gating signal for *k* FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate (ICG). Such data-driven gating is used for a digital filter in an ultralow-power design. A single ICG is amortized over *k* FFs. There is a clear tradeoff between the number of saved (disabled) clock pulses and the hardware overhead. With an increase in *k*, the hardware overhead decreases but so does the probability of disabling, obtained by ORing the *k* enable signals.

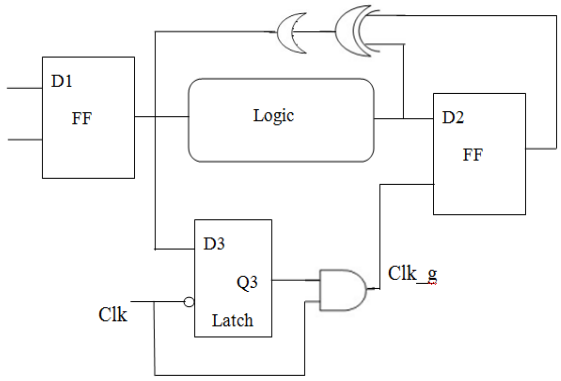

Fig. 3 Data driven clock gating

Advantages

Data-driven gating aims to disable large amount of redundant clock pulses. To reduce the hardware overhead, flip-flops are grouped so that they share a common clock enabling signal [2].

Disadvantages

Data-driven gating suffers from a very short time-window where the gating circuitry can properly work. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF.

C. Auto-gated Flip-flops

The basic circuit used for Auto-Gated Flip-Flip (AGFF) illustrated in Fig. 4. The FF's master D latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master D latch becomes opaque and the XOR gate indicates whether or not the slave D latch should change its state [4]. If it does not, its clock pulse is stopped and otherwise it is passed. A significant power reduction was reported for register-based small circuits, such as counters, where the input of each FF depends on the output of its predecessor in the register.

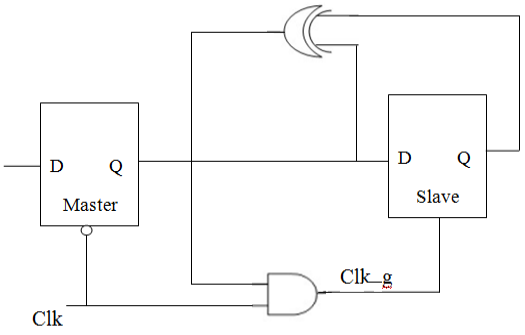

Fig. 4 Auto gated Flip-Flops

Advantages

Auto-Gated Flip-Flip (AGFF) method is very simple to implement and can be used for general logic by allotting a full clock cycle for the computation of the enabling signals and their propagation.

Disadvantages

AGFF has two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

IV. Look Ahead Clock Gating Technique

Look Ahead Clock Gating (LACG) overcomes all the disadvantages of previous clock gating technique which is shown in the Fig. 5. LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation [3].

LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in to generate clock enabling signals of other FFs in the system, whose data depend on that FF.

The full clock cycle is allotted for the computation of the clock enabling signals and their propagation. The glitches occur in the previous clock gating methods like data-driven clock gating, auto gated flip-flops can be eliminated with the help of the look ahead clock gating technique.

LACG is independent of the knowledge of the flip-flops data toggling vectors and it is capable of stopping the majority of redundant clock pulses. The LACG logic can be easily derived from the underlying RTL functional code as it significantly simplifies the gating implementation.

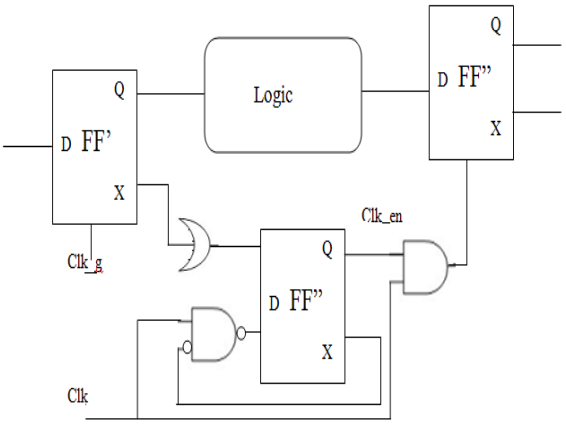

Fig. 5 Look Ahead Clock Gating Technique

V. Proposed Lfsr with Lacg Technique

Clock signal is a great source of power consumption because of high frequency and load. Clock signal is not carrying any information. Gating the clocks can lead to save the power by reducing unnecessary clock. AND gate is hardly used to gate a clock that is active on the rising edge.

LFSR is the most used topology to implement PRBG. It is obtained with an array of FFs with a linear feedback performed by several XOR gates. This project presents the look ahead gated clock design approach for LFSRs [8] which can lead to power reduction without unduly complicating the traditionally simple topology.

To show LACG technique is best, the comparison is made between LFSR with data-driven clock gating and LFSR with LACG technique. The power values are also compared to the conventional LFSR. In data-driven clock gating there exist a serious timing problem for large applications but in LACG technique, the timing problem doesn't exist because of the full clock cycle allocation to determine the clock enable signal.

To reduce the hardware overhead, the FFs in the LFSR can be grouped so that, they share common clock enable signal. Extra logic and interconnections are needed to generate the clock enabling signals, and resulting area and power overhead must be considered. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. The optimal fan out of a clock gater yielding maximal power savings is derived based on the average toggling statistics of the individual FFs.

The schematic of Look Ahead Clock Gating in 16-bit Linear Feedback Shift Register is shown in the Fig. 6. The proposed technique consists of two inputs namely enable and reset. The input to the LFSR is denoted as D[n] and the output is denoted as Q[n]. The clock input is given to the integrated clock gating cell and the gated clock is given to the clock input of all flip-flops. The enable signal is given to the AND input which is then given as input to the D-latch.

In normal D flip-flop, the output Q reflects back the input D. The basic D – Flip flop works based on the clock. When the clock signal is enabled, the input of the D flip-flop is given to the output. Due to this reason even for the same value of input, the clock signal is repeatedly doing its function, thus makes more consumption of dynamic power.

In LACG technique, the comparison between input D and output Q is done by an XOR gate which feeds the AND gate to produce the required gated clock (GC) signal for the latch. When both D and Q are the same, the gated clock signal will remain low and will not consume power for switching. When they differ, the gated clock signal will copy the original clock and may make a necessary transition to change the state of the latch.

LACG achieves better reduction in dynamic power by reducing the switching activity of clock signal. A normal 4-bit LFSR output say 1100, needs four clock cycles to get the four bit inputs. But in LACG technique, it needs only 2 clock cycle because it compares the adjacent bits using XOR gate. If the input and output bits are same then there is no clock signal but in case if the input and the output bits are different then the clock signal is applied to the circuit.

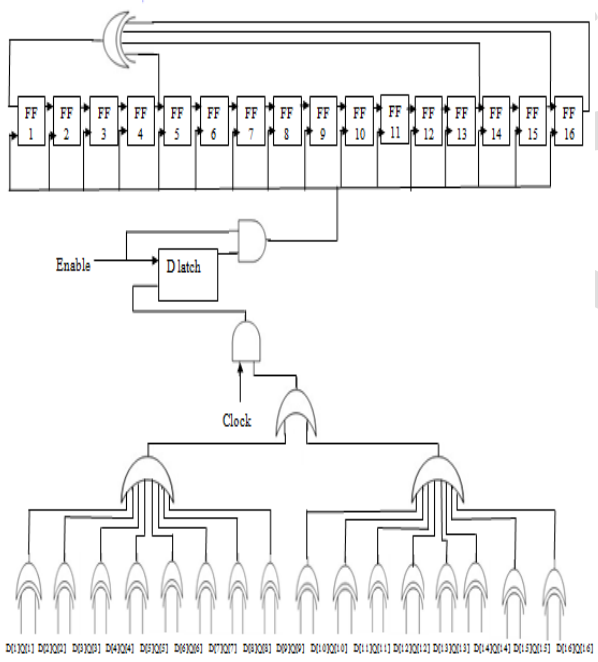

Fig. 6 Schematic of LFSR with LACG Technique

From Fig. 6, it can be inferred that the XOR operation is performed between 4th, 13th,15th and 16th registers because the characteristic polynomial of 4 – bit linear feedback shift register is $1+x^4+x^{13}+x^{15}+x^{16}$. For 16–bit LFSR, the maximal length sequence is $2^{16}-1=65535$ hence this shifting operation is performed up to 65535 clock cycles and after 65535 cycles the operation restarts.

TABLE I. TRUTH TABLE FOR SINGLE D FLIP-FLOP WITH LACG

Clk	D	Q	Y (output of XOR)	GC (output of AND)
+ve	0	0	0	0
+ve	0	1	1	1
+ve	1	0	1	1
+ve	1	1	0	0

VI. SIMULATION RESULTS

A novel Linear Feedback Shift Register (LFSR) with Look – Ahead Clock Gating (LACG) is designed to reduce the dynamic power consumption. The simulation results and the power consumption values for the proposed technique are achieved using the simulation tool called CADENCE. A CADENCE design system is Electronic Design Automation (EDA) software which produces software and hardware for designing integrated circuits, System-On Chip (SOC) and printed circuit boards. The LACG technique is initially applied to single D flip-flop and the better power reduction is achieved. Then, the LACG technique is further applied to 4-bit, 8-bit, 16-bit and 32-bit LFSR. The power consumption values for the various bits of LFSR's are compared with the conventional LFSR and LFSR with the data-driven clock gating technique to show better power savings.

The Simulation result for 4-bit LFSR with LACG is given in Fig. 7. The input and output to the LFSR is denoted as d [3:0] and q [3:0]. The other two inputs given to the LFSR are clock and reset signal which is denoted as clk and en. K [3:0] represents the output of XORs which is used for comparing the input and the output. The output of OR is denoted as g, which is used to group the output of all XORs. The output from the ICG cell together with the AND gate is denoted as gc, which is the gated clock signal. The term temp is used to denote the switching activity of clock which is very low compared to the ordinary clock signal. It indicates that after applying LACG technique, the activity of clock signal gets reduced thus achieving reduction of dynamic power.

Similarly, the simulation results for 8-bit, 16-bit and 32-bit LFSR with LACG is shown in Fig. 8, Fig. 9 and in Fig. 10.

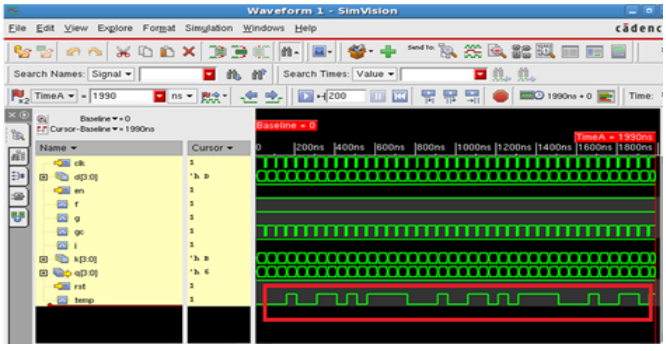

Fig. 7 Simulation result for 4-bit LFSR with LACG

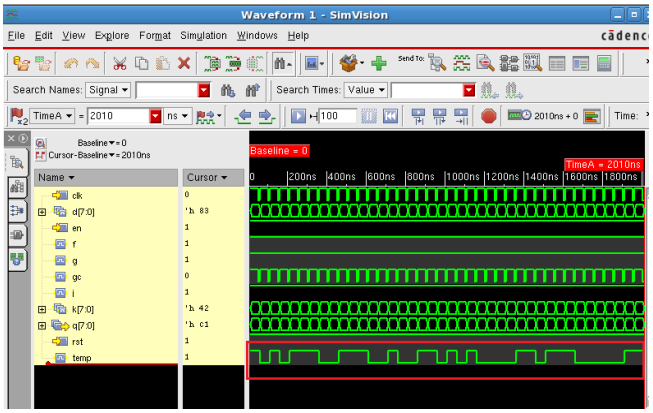

Fig. 8 Simulation result for 8-bit LFSR with LACG

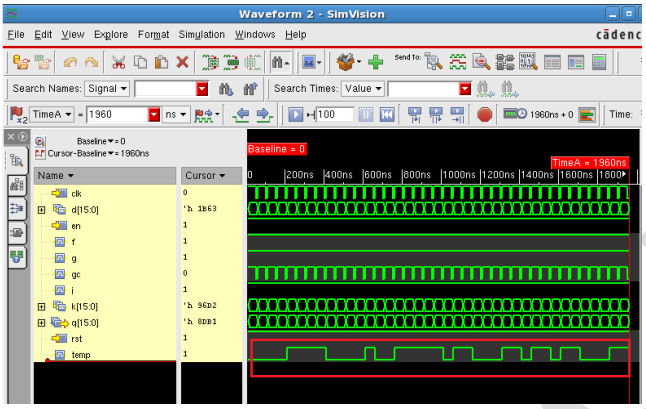

Fig. 9 Simulation result for 16-bit LFSR with LACG

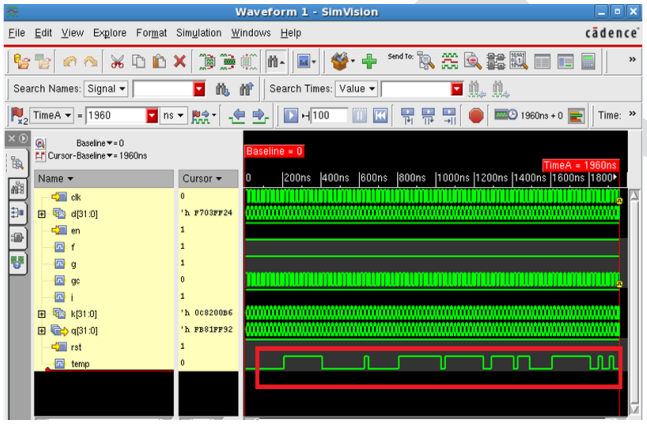

Fig. 10 Simulation result for 32-bit LFSR with LACG

The power consumption values for conventional LFSR, LFSR with data-driven clock gating and LFSR with LACG technique for different bits is shown in table II.

From table II, it is observed that when compared to conventional 1-bit FF and 1-bit FF with data-driven clock gating the proposed FF with LACG technique achieves power savings on an average of 90.53%. Similarly, when compared to 4-bit conventional LFSR and LFSR with data-driven clock gating the proposed LACG technique achieves power savings of 83.43%. For 8-bit LFSR, proposed LACG technique achieves power savings on an average of 81.25%. For 16-bit LFSR, power savings of 81.49% is achieved using LACG technique. Similarly, for 32-bit LFSR power savings of 79.58% is achieved using LACG technique.

TABLE II. COMPARISON OF POWER CONSUMPTION VALUES OF VARIOUS LFSR WITH DIFFERENT CLOCK GATING TECHNIQUE

No. of. Bits	Conventional LFSR (without any clock gating)	LFSR with Data Driven Clock Gating	LFSR with Look Ahead Clock Gating	% of Power Savings
1 bit	6581.85nW	8253.161nW	5958.673nW	**90.53**
4 bit	30109.909nW	43516.238nW	25120.25nW	**83.43**
8 bit	69645.476nW	84701.377nW	56589.673nW	**81.25**
16 bit	128452.666nW	163685.692nW	104681.463nW	**81.49**
32 bit	257788.967nW	343043.317nW	205150.688nW	**79.58**

The power comparison values for the LFSR with LACG, LFSR without LACG and LFSR with data-driven clock gating using CADENCE is shown in the Fig. 11.

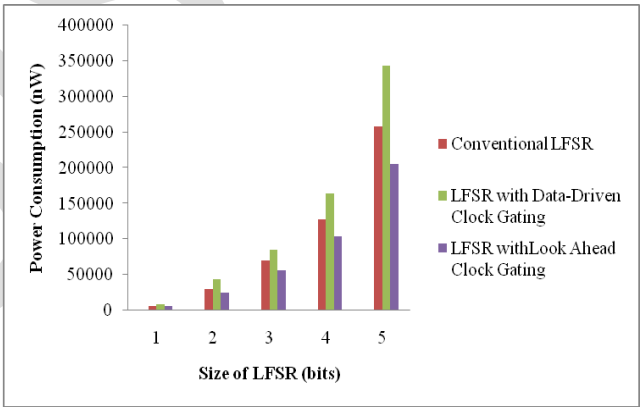

Fig. 11 Power comparison for LFSR

From Fig. 11, it is clear that the proposed LFSR with LACG achieves better power reduction compared to the conventional LFSR and LFSR with data-driven clock gating. The power consumption of 32 – bit LFSR is about 257788.967nW and the power consumption of 32 – bit LFSR with data-driven clock gating is about 343043.317nW. Using LACG technique the power consumption has reduced to 205150.688nW.

VII. CONCLUSION

The simulation results clearly show that the proposed design has much less dynamic power compared to the ordinary LFSR without clock gating technique and to the data-driven clock gating technique. The dynamic power values for the 4-bit, 8-bit, 16-bit and 32-bit LFSR with LACG is simulated using CADENCE. The power savings on an average of **81.44 %** is achieved using the novel Linear Feedback Shift Register

design with Look Ahead Clock Gating technique. The proposed LFSR with LACG will be very effective for the applications like Built-In Self Test (BIST), cryptography and in spread spectrum communication system.

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