FPGA Based SPWM Technique for a Three-Level Inverter

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***Abstract*- This paper is about the design and implementation of a FPGA Controller based Sinusoidal Pulse Width Modulation (SPWM) Technique for a Three Phase Three-level Inverter using VHDL. The generated pulses can be used for the Induction Motor speed control. In the past years DC motors were very popular in variable-speed drives. Today DC motors are being replaced by AC motors with associated converters, because the converters are becoming cheaper. AC drives use an adjustable-frequency inverter that adjusts frequency and voltage to vary the speed of an AC motor. This control is typically produced through pulse width modulation (PWM). Today FPGAs are alternative to DSPs. Since the FPGA is suitable for fast implementation control and can be programmed to do any type of digital functions. The FPGA based controller is used to generate SPWM pulses using VHDL for Voltage/ frequency (V/f) control, which is used to control the Inverter. The output of the inverter can be used as supply to a three phase induction motor and thereby speed of the motor can be controlled. SPWM is a very simple technique for harmonic reduction. In this technique pulse magnitude will be constant and only pulse time (width) can be changed. In this technique pure sine wave is compared with carrier (triangular) wave and produces gate pulses.**

Keywords- SPWM, FPGA, VHDL Code, Three-level inverter.

I. INTRODUCTION

Pulse Width Modulation has nowadays become an integral part of every electronics system. These techniques have been widely accepted and are researched extensively nowadays. It has found its application in large number of applications as a voltage controller. Its use in controlling output voltage of Inverter is the most frequently used application. This paper has included about Three Level Inverter (Neutral Point Clamped Three Level Inverter)which is used to convert uncontrolled D.C. in to controlled A.C. using Sinusoidal Pulse Width Modulation (SPWM) technique which is widely used in industrial applications like speed control of Induction Motor, Brushless D.C. Motor etc. The digital logic to implement a full featured PWM unit for three level inverters that determines all required switching sequences and the necessary blocking times can be fitted together with FPGA. Due to the straight forward VHDL, the solution is extremely fast and allows a cost-efficient single chip implementation even for very high switching frequencies [2].

Generally, an 8-bit microprocessor can handle most of the necessary computations. Microprocessor based controllers are more economical, but often face difficulties in dealing with control systems that require high processing and input/output handling speeds. Rapid advances in digital technologies have
given designers the option of implementing a controller on a variety of Programmable Logic Device (PLD), Field Programmable Gate Array (FPGA), etc. FPGA is suitable for fast implementation controller and can be programmed to do any type of digital functions. There are three main advantages of an FPGA over a microprocessor chip for controller designing:

- An FPGA has the ability to operate faster than a microprocessor chip
- The new FPGAs that are on the market will support hardware that is upwards of one million gates, which increase program capacity
- Because of the flexibility of the FPGA, additional functionality and user interface controls can be incorporated into the FPGA minimizing the requirement for additional external components

FPGAs are programmed using Very High Speed Integrated Circuit hardware description language (VHDL). Once they are programmed, they can be disconnected from the computer, and it will be running as standalone device. The FPGAs can be programmed while they run, because they can be reprogrammed in the order of microseconds. This short time means that the system will not even sense that the chip was reprogrammed. Applications of FPGAs include industrial motor drivers, real time systems, digital signal processing, aerospace and defense systems, medical imaging, computer vision, speech recognition, cryptography, computer hardware emulation and a growing range of other areas.

II. NPC THREE- LEVEL INVERTER

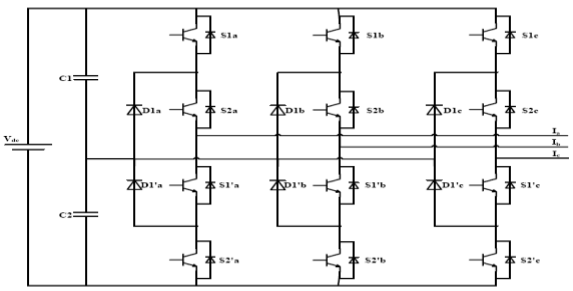


Fig 1 : Schematics of a 3-level npc Inverter using IGBT Modules

Nowadays in so many applications desire controlled A.C. for controlling speed of machines like Induction Motor,

Brushless D.C. Motor etc. Inverter is converting uncontrolled D.C. in to controlled A.C. There are so many types of inverter like two level, three level and five level etc. In this paper three level inverter has discussed and it's results.

Three level inverter has made up of D.C. source, twelve power electronic devices (IGBTs), six clamping diodes, and two capacitors. Sinusoidal Pulse Width Modulation (SPWM) technique is used to generate the gate pulses. SPWM technique is widely used in industries. Neutral point clamped Three Level Inverter is the modified version of Three Level Inverter also discussed in this paper [2].

Driven by products from the fields of renewable energies and uninterruptible power supplies (UPS), different manufacturers of power electronics components now offer IGBT modules in which an entire three-level phase is integrated. Three-level topologies have been standard for applications in the MW range for many years. The main reason behind this is the much lower blocking voltage capability that the power electronic switches must exhibit.

The switching operation of npc three-level inverter is given below :

- Turn on upper switches, S_1 and S_2, in order to obtain $V_{an} = +V_{dc/2}$
- Turn on middle switches, S_2 and S_1**'**, in order to obtain $V_{an} = 0$
- Turn on lower switches, S_1' and S_2', in order to obtain $V_{an} = -V_{dc/2}$

III. CONTROL TECHNIQUE OF THREE LEVEL INVERTER

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications. The fundamental frequency SPWM control method was proposed to minimize the switching losses. The multi-carrier SPWM control methods also have been implemented to increase the performance of multilevel inverters and have been classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD), while horizontal arrangement is known as phase shifted (PS) control technique.

The mentioned multi-carrier SPWM control technique has been illustrated in Fig 2. The sinusoidal SPWM is the most widely used PWM control method due to many advantages including easy implementation, low switching losses. In SPWM control, a high frequency triangular carrier signal is compared with a low frequency sinusoidal modulating signal in an analog or logic comparator devices. The frequency of modulating sinusoidal signal defines the desired line voltage frequency at the inverter output [6].

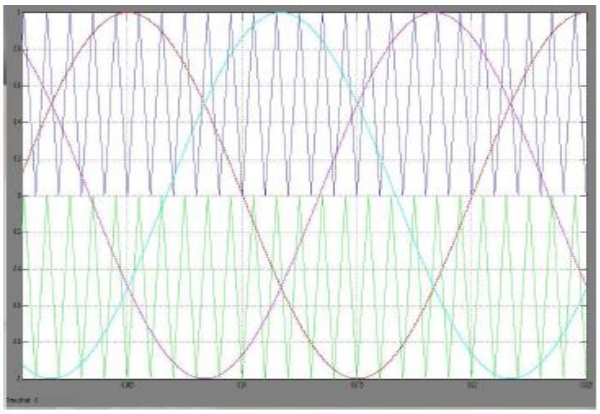


Fig. 3: SPWM control strategy for three-level inverter

The sinusoidal PWM technique is very popular for industrial converters. Following figure shows the general principle of SPWM, where an isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave, and the points of intersection determine the switching points of power devices. Three level pulse width modulated waveforms can be generated by sine carrier PWM. Sine carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves [3].

$V_{io} = V_{dc/2}$, $V_{ref,i} > V_{tri,1}$

$= 0$, $V_{tri,1} > V_{ref,i} > V_{tri,2}$,

$= -V_{dc/2}$, $V_{tri,2} > V_{ref,i}$

where i = a, b or c

The three reference control signals are phase shift 120^0 each other with same amplitude. Two carrier waves are in phase each other with dc voltage offset. Two important parameters of the design process are amplitude modulation index $m_a = V_r / V_c$, where V_r is the amplitude of reference control signals, V_c is the peak amplitude of the carrier wave, and the frequency modulation index $m_f = f_c/f_r$ where f_c is the frequency of the carrier wave and f_c is the carrier frequency.

IV. FIELD PROGRAMMABLE GATE ARRAY

FPGAs stand for Field Programmable Gate Arrays are one type of programmable logic devices (PLDs). They are an integrated circuit that can be configured by the user in order to implement digital logic functions of varying complexities. FPGAs can be very effectively used for control purposes in processes demanding very high loop cycle time. One of the fundamental advantage of FPGA over DSP or other microprocessors is the freedom of programming parallelism. Since different parts of FPGA can be configured to perform independent functions simultaneously, its performance is just not tied to clock rate as in DSPs. This fact enables FPGA's to score over general purpose computing chips in the digital control systems implementation.

V. CALCULATIONS FOR GENERATING THE SINE AND TRIANGULAR WAVES

1. *Generation of Triangular carrier signal of 10KHz*
   This Up Down counters are used to generate Triangle signal
   Counter counts for each clock cycle of 50ns
   To get the frequency of 10 KHz each cycle $:= \frac{1}{10000} = 100us = 100000ns$
   Therefore up/down counter is for $\frac{100000ns}{2} = 50000ns$
   The count value $\frac{50000ns}{50ns} = 1000$ counts
2. *Generation of Sine wave*
   Sine wave is generated by Lookup table method
   Sine data for 360 degrees is stored in 256 locations each of size 9 bits including sign bit
   Sin 0=0
   Positive peak value is sin 90 =1 for 9 bits it is equal to 255
   Negative peak value is sin 270=-1 for 9 bits it is equal to -255

   A Ramp signal is generated by the up counter to take the samples of sine data from look up table. Samples are taken based on the frequency step applied.

3. *Frequency step calculation*
   Example for 50Hz sine wave with Sampling frequency=10 KHz
   It means that 100000 samples are taken in one second
   For 50 Hz the number of samples required for one full cycle of sine wave is equal to $\frac{10000}{50} = 200$ samples
   After 200 samples the signal has to repeat for this we need another ramp signal (i,y and b of program in appendix)of 0 to 255 to point 256 locations
   Therefore frequency step $\frac{256 * 256}{200} = 327$
   To get 3 phases of 120 degree phase displacement Refer appendix program
   Ramp signal is from 0 to 255
   255/3=85
   Ramp signal i starts from 0
   Ramp signal y starts from 85
   Ramp signal b starts from 170
   Magnitude can be varied by multiplying with an integer value.

4. *PWM Generation*
   PWM signals are generated by comparing magnitudes of each sine wave form with carrier signal.

The program is developed on Xilinx 13.1 software in VHDL language. The program is verified with Modelsim simulator. Model sim has the feature of forcing clock and other inputs. The following are the graphs obtained for different values of inputs (amplitude and frequency)

VI. MODELSIM RESULTS

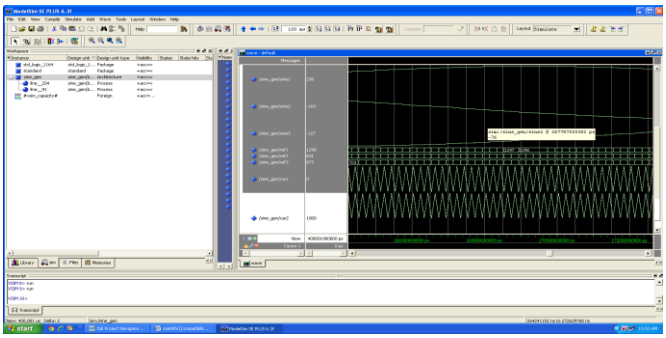


Fig. 4: triangular waves

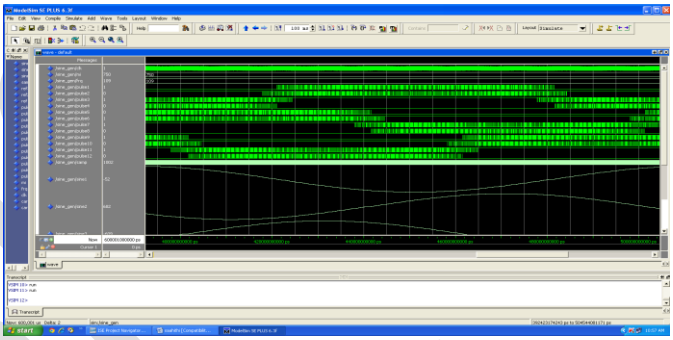


Fig. 5: three phase sine waveform

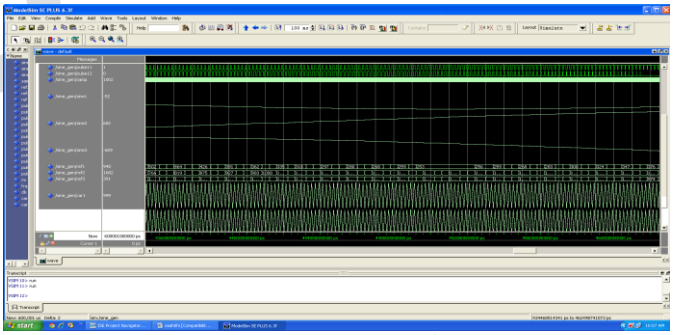


Fig. 6: sine and triangle waveforms

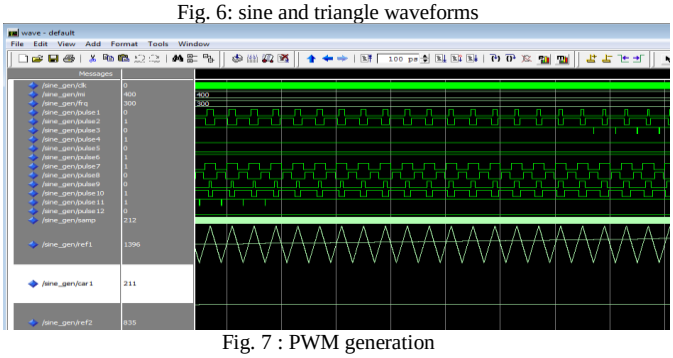
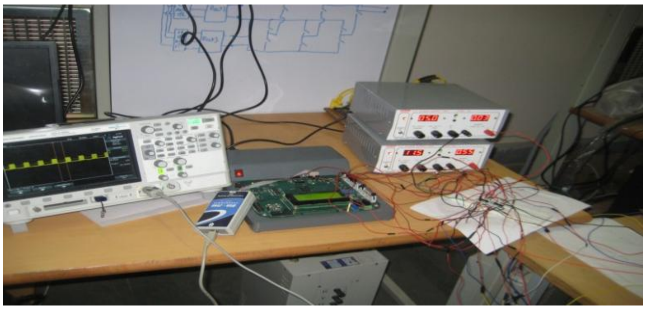


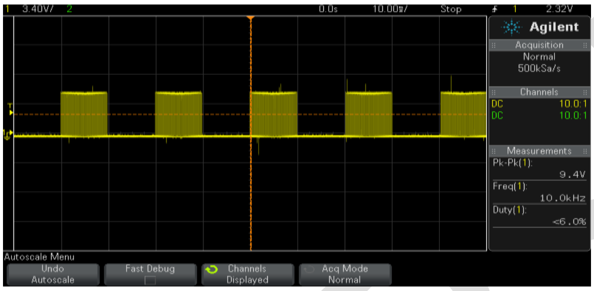
Fig. 7 : PWM generation

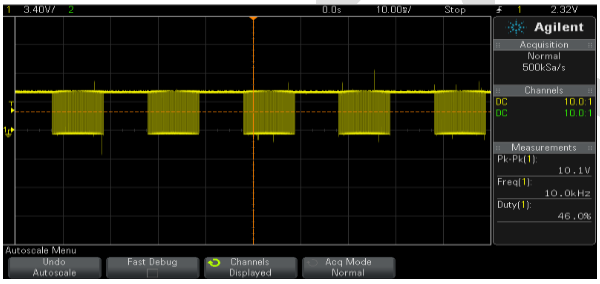
VII. SOME PRACTICAL ASPECTS

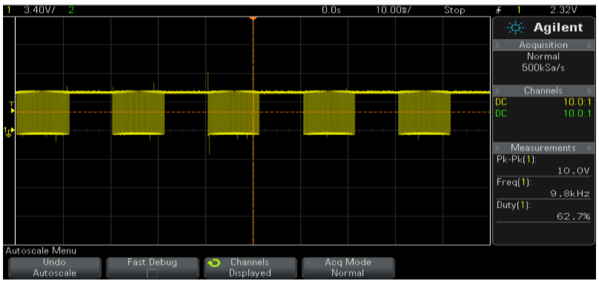


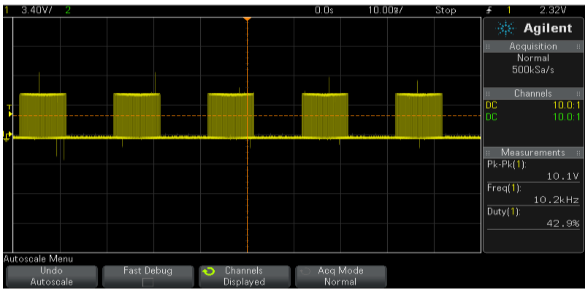
To conduct the experiment the necessary DC voltage is taken through Auto transformer and the bridge rectifier with the filter capacitor. The programmed FPGA kit is connected to the gate driver circuit through buffer to increase the voltage from 5v to 12v. The PWM signals from the kit are first verified with the CRO for different frequency and different amplitudes of the modulating signal. The dead band required is allotted in the program itself.

CRO Results









VIII. CONCLUSIONS

Sine- triangle wave forms are generated and their comparison also done for the PWM to be generated using VHDL coding using Xillinx ISE 13.1 soft ware. Code then downloaded into SPARTAN-6 FPGA board and verified the generated PWM signals in the CRO. Since FPGA board output pins voltage is 5 volt, the voltage is increased to 12 volt using buffer circuit. Then the PWM signals are given to the gates drivers of inverter module and tested.

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