Degradation Mechanisms and Lifetime Modeling of Power Semiconductor Devices

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Abstract: **Lifetime modeling and predicting for power semiconductor devices has become important due to higher demands on reliability and economy, i.e. to save time and money. Understanding the degradation mechanisms of such devices in a complex interplay of thermal, mechanical, and electrical loading in often harsh environment is a very challenging task, involving the competences of electronic engineers, simulation experts, materials scientists, physicists and mathematicians - with the final goal to permit accurate prediction of failure probabilities in the ppm-range as a function of time. In this review paper, I've discussed previously published literature on degradation mechanisms, experimental results obtained in several studies, lifetime prediction procedure, lifetime model and some preventive measures that can be taken against permanent damage.**

Key-words: **Degradation mechanism, Semiconductor lifetime, linear models, Bayesian regression**

I. INTRODUCTION

Since the invention of uncommon semiconducting behaviors of Si and Ge, a lot of semiconductor devices have been playing a diversified role on our modern life. Switching, amplifying, energy conversion, modern communication devices including display devices are some examples. In the beginning times, these devices were carefully modeled and structured from theoretical level to the industrial or implementation level. With the advancement of time and the growing needs for fashionable as well as dynamic consumers, those devices have been upgraded to mini, micro and even nano level. Traditional BJT has been upgraded to TFT, then Organic structure. As the models, mechanisms, technology are increased, same is the acute competition among the investors or manufacturers. Despite (careful model/design, fabrication method), there're questions on device reliability-how long they sustain, or how fine is performance. After having finished an attractive performance, some devices become fractured, shorted or burned or even decomposed (electronic waste) as well as their inside mechanisms. There're some other dimensions of device degradation also.

The power semiconductor devices have been grouped into following two categories:

i. The old or conventional devices i.e. power diode, thyristor, TRIAC, GTO, BJT and power MOSFET.
ii. Modern power devices i.e. IGBT, SIT, SITH, MCT, IGCT and COOLMOS etc.

II. MECHANISMS AND MODELING OF DEGRADATION

Inside the structures and fabrication processes

Oxidation, radiation (both natural and man-made), and chemical degradation of the dielectric, and probably several other aspects, degrade the ICs over time. The effect of these influences largely depends on the manufacturing process and the quality of the IC.

Failures can be caused by excess temperature, excess current or voltage, ionizing radiation, mechanical shock, stress or impact, and many other causes. In semiconductor devices, problems in the device package may cause failures due to contamination, mechanical stress of the device, or open or short circuits

Before analyzing the degradation of any device, let's have a look inside the device structure and fabrication process. Development of physical degradation models

- Stress test data analysis
- Technology- and product understanding
- Use of numerical electro-thermal and thermo-mechanical simulation

Finite Element Method (FEM) is widely used in several engineering disciplines because of the tremendous increase in computer power and commercially available FEM tools. Nowadays, large scale simulations with several millions of degrees of freedom (DOF) are possible. Modeling not only reduces the cost and time in design cycles, but also plays a vital role in understanding the fundamental behavior of the system, especially in the microelectronics industry, where the spatial dimensions are in the range of micrometers to nanometers.

The main goal is to reproduce all occurring electrical and thermo-mechanical phenomena arising during the manufacturing processes of integrated power semiconductors as well as during field application as efficiently as possible. Hence, 3D simulations are performed in addition to 2D design studies.

Fig.1 Typical physical fracture of devices.

State-of-the-art use of physical analysis

In this method some defected or degraded samples are collected and observed. Then their individual and circuit level defects are experimented, clearly considering the ideal or factory-designed model and time of manufacture. Then calculating the numbers of defected or degraded items per sample and manipulating percentile value, we can guess a rate of degradation or malfunction etc.

- Optical-, Electron-, Scanning Acoustic and X-ray microscopy

Advanced image analysis

Development of degradation-mode oriented stress testing

- Adaption and enhancement of electrical stress test concepts
- Development of test structures and test benches for thermo-mechanical fatigue analysis
- Infrared thermography and laser vibrometry (more details: Material Characterization
- Statistical data analysis and lifetime models
    - Lifetime modeling and prediction methods for unimodal and multimodal distributions with censored data, (Bayesian) Regression, Mixtures-of-Experts models, Bayesian Networks and Gaussian Processes, accelerated lifetime models and bi-variate distributions Statistical evaluation methods for model and prediction quality
- Stochastic degradation modelling
    - Stochastic processes to model degradation in semiconductor devices
    - Stochastic State-Space-Models

$$\frac{\partial}{\partial t}U(t,x) = \nabla.(1/2(\nabla.((b^{\theta}\,(b^{\theta})^{T})(t,x)u(t,x) - a^{\theta}(t,x)u(t,x))$$

$$\frac{\partial}{\partial t}U(t,x) = -\nabla.J^{\theta}(t,x))$$

Objectives/Procedures: Analyze and identify the degradation processes taking place in different layers of semiconductor devices under electro-thermal loading conditions and clarify their relevance for device functionality

- Identify suitable load- and strength related parameters which permit quantification of degradation and resistance in experiments and numerical simulation
- Develop mathematical and statistical models which describe degradation and permit lifetime prediction – and provide a mathematical framework of stochastic state space modeling to capture variations in lifetime.
- Develop and test new solutions in product- and technology design with improved reliability.

Degradation of Electrical Parameters

There are a few different ways to characterize a silicon-based semiconductor: electrical characterization, optical characterization, and the physical/chemical characterization. Electrical characterization helps to determine the resistivity, carrier concentration, mobility, contact resistance, barrier height, depletion width, oxide charge, interface states, carrier lifetimes, and deep level impurities. Two-point Probe, Four-point probe, differential Hall Effect, Capacitance-Voltage Profiling, DLTS, and DlCP.

Linear Model/Bayesian Model for Degradation Analysis and Prior Selection Selecting the prior distribution is essential for Bayesian inference. In this work a set of uninformed and informed priors is used. Uninformed means that no knowledge about the parameters is given, informed means knowledge, e.g. mean and standard deviation, from given data or from experts is available.

Possible distributions for the β_is are the following:

- diffuse normal: $\beta_i \sim N(0, 10^6)$
- informed uniform: $\beta_i \sim U(m_i - 3 * s_i, m_i + 3 * s_i)$
- informed normal: $\beta_i \sim N(m_i, s^2)$
- non centralized student t with 1 df: $\beta_i \sim nct(m_i, 1)$
- gamma or negative gamma distributions: $\beta_i \sim \pm Gam(a_i, b_i)$

The prior information for the means $\underline{m}$ =(6.71, 13.85, 23.88, 16.41, 6.28) and the standard deviations $\underline{s}$ = (0.13, 1.04, 1.65, 1.15, 0.93) of the model parameters are extracted from the given data.

When normal priors for the β_is and an inverse gamma (IG) prior for σ^2 are used, than the resulting posterior distributions for the parameters can be calculated analytically ($\beta_i / \underline{y} \sim t$ and $\sigma^2/\underline{y} \sim IG$), but in all other cases the posterior distribution needs to be simulated numerically. This has been done with the slice sampling algorithm in MATLAB, with a sample size of 10000 and a burn in period of 1000.

Model Definition After selecting the prior the full Bayesian LM can be defined as: $\underline{y} \sim N(\underline{\mu}, \sigma^2 I)$

$$\underline{\mu} = X\underline{\beta} + \epsilon$$

$$\beta_i \sim N(m_i, s_i)$$

$$\sigma^2 \sim IG(a, b)$$

Bayesian law converts to: $p(\theta|\underline{y}) \propto \boldsymbol{L}(\theta|\underline{y}) \cdot p(\theta)$

This equation shows that the joint posterior distribution of data and model parameters is proportional to the likelihood times the prior distribution of the parameters. Integrating the specific joint posterior distribution of the model defined in equation 7 with respect to $\underline{\beta}$ and σ^2, respectively, leads to student t distributions for the β_is and to an inverse gamma distribution for σ^2. The summary statistics for the model parameters are given in table 1.

Table 1: Summary statistics of posterior distributions

parameter	mean	st.dev	Quantiles 5%	95%
β_0 (intercept)	6.71	0.08	6.58	6.84
β_1	-13.82	0.91	-15.30	-12.32
β_2	-24.03	1.14	-26.02	-22.21
β_3	-16.38	0.73	-17.61	-15.22
β_4	6.38	0.54	5.54	7.29
σ^2	0.71	0.05	0.64	0.79

The standard deviations of the model parameters vary between 1-8% of the mean and the percentages of the simulation errors are in the same range, this means that simulation results are reliable, although they might be improved since<5% simulation error is desired.

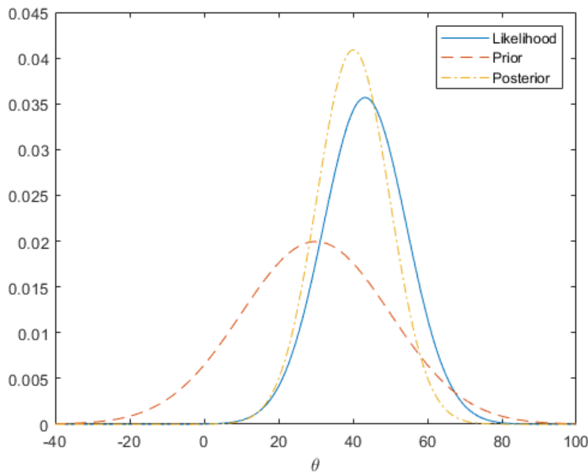

Fig.2-Bayesian model plot

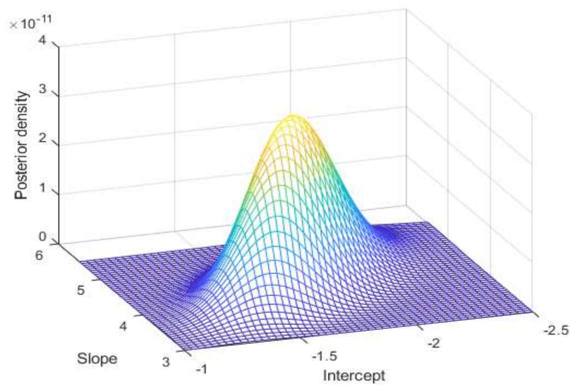

Fig.3- Posterior vs intercept of Bayesian data.

This posterior is elongated along a diagonal in the parameter space, indicating that, after we look at the data, we believe that the parameters are correlated. This is interesting, since before we collected any data we assumed they were independent. The correlation comes from combining our prior distribution with the likelihood function.

This work showed that modeling the lifetimes of power semiconductor devices with Bayesian LMs is possible, but restricted to a specific range, where tested devices have the same failure mechanisms. Expanding the prediction range showed the poor extrapolation quality of the model for tests with probably other failure mechanisms. As a step of improvement a Bayesian LM with mixed distributions was used[2], but no significant increase in quality could have been observed, hence further improvements and/or other model assumptions are needed.

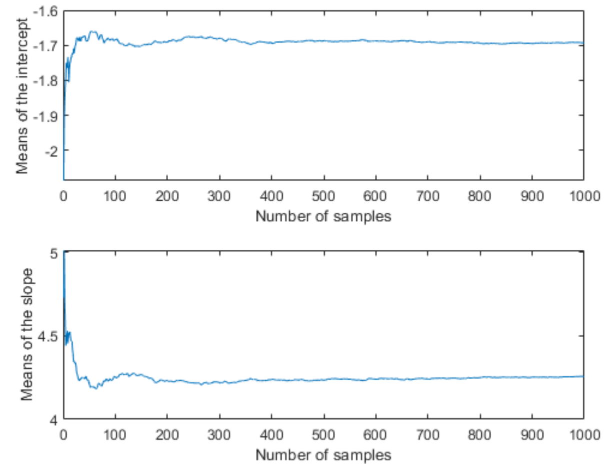

Fig.4-Bayesian model sample analysis

It appears that the sample size of 1000 is more than sufficient to give good precision for the posterior mean estimate.

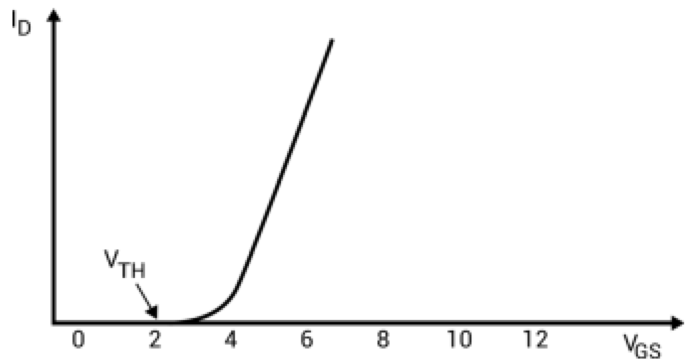

Fig.5 Gate-to-source voltage vs. drain current characteristics for power MOSFET

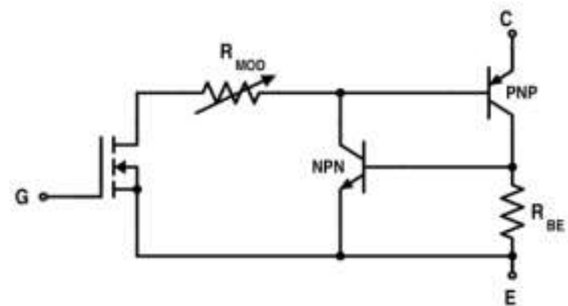

Fig.6 Equivalent circuit for IGBT

Lifetime Prediction Procedure

The major parts of the lifetime estimation procedure of power semiconductor devices are shown in a flow chart diagram[6].Based on a given mission profile, which contains operation information like mission time t_{mis}, phase current, battery voltage, switching frequency etc., temperature profile of the power semiconductors $T_j(t)$ can be calculated. Since power loss of the semiconductor device $p_V(t)$ depends on its temperature, the calculation of the power loss and the temperature of semiconductor devices is normally performed in an iterative way, until the point of convergence is reached. By using cycle counting method as for example shown in [16], the corresponding temperature profile can be reduced into a set of repeated single stress conditions with corresponding cycles N, which include lifetime-deciding information like junction temperature swing ΔT_j, mean junction temperature T_{jm} and load pulse duration t_{on}. For each single stress condition, the expected time to failure N_f can be calculated with lifetime models, such as [17], [18], and [19], which are normally based on results from a plenty of power cycling tests. The damage of all single stress conditions is then cumulated linearly to the total damage Q according to the Miner's rule [20]. If the sum of the lifetime consumption reaches one, the total lifetime limit is then considered to have been reached [21].

There are in total five main steps in the lifetime estimation procedure of power semiconductor devices:

1. Power loss calculation based on mission profile.
2. Thermal calculation based on power loss calculation results and system thermal behavior.
3. Lifetime modelling using power cycling test data.
4. Temperature cycle counting for damage calculation.
5. Calculation of total damage based on linear cumulative damage rule.

The development and innovation of power semiconductor devices are becoming faster, which means that products must be brought to the market quicker to meet the rapid changes in the market. At the same time, the expectation and requirement of the quality and reliability of power semiconductor devices have even become higher. In order to accomplish this seemingly impossible mission, manufacturers of semiconductors must assure long operating periods with high reliability but in a short time. Most commonly used solution is the accelerated test.

Lifetime Model

The lifetime models of power semiconductor devices are usually made based on physical or empirical approaches. For a physical approach as for example shown in [22], a well understanding of the material and device properties as well as the physic of the failure and the process of deformation is a must. The lifetime prediction base on the physical approach is usually done by calculating the stress strain deformation of certain components, which could be gained either by experiments or simulations. Since the power semiconductor devices have an extreme complicated multi-physical system, where the electrical, thermal, and mechanical characteristics are strongly coupled together, it is quite hard to fully manage the internal processes of the power semiconductor devices during the aging. Certain simplifications are usually made in order to propose a physical lifetime model. Thus, it is difficult to accomplish a high accuracy and a wide range of applicability at the same time.

For the lifetime of a certain material or component, several empirical lifetime models have already been published before the time of power semiconductor devices. The most well-known model is the Coffin-Manson relationship for the acceleration of fatigue under thermal cycling condition. The number of cycles to failure N_f based on Coffin-Manson relationship is given:

$$N_f = K \cdot \Delta T^{\alpha}$$

where K is the basic lifetime, ΔT is the temperature swing, and α is the Coffin-Manson exponent. The Coffin-Manson relationship was published by Coffin in 1953 [23] and Manson in 1954 [24] independently for describing the effect of thermal cycling stress on the lifetime.

It is obvious that the Coffin-Manson approach is too simple for a complex system and several other effects (like for example temperature, pressure or humidity) are not taken into consideration. The practical experiences have often shown that the lifetime of components is decreasing with increasing absolute temperature, as it is given by the Arrhenius equation [25] circuits was published by Norris and Landzberg to characterize the fatigue due to thermal cycling with considering its thermal cycling frequency f [26]

The research on lifetime model of IGBT power modules has started in the late 1990s. The first two projects were mainly focusing on the power cycling capability of IGBT in power module packaging, namely the Swiss project

Lifetime Modelling

In the test 1, 1200 A rated current IGBTs and diodes from two different manufacturers were tested with load pulse duration t_{on} = 1 s, cooling phase duration t_{off} = 2 s, coolant inlet temperature T_{inlet} = 50°C and coolant flow rate per heat sink $\dot{V}$ = 6 – 7 l/min.[6]

The gate voltage V_{GE} of IGBTs from manufacturer B was reduced to 12.5 V to further increase their power losses. Therewith, the difference of load current between three power paths was reduced. After the adjustment of test conditions in the start-up phase, the initial setting of test (t_{on}, t_{off}, I_L, V_{GE}, Tinlet and $\dot{V}$) was kept until the end of test

III. CONCLUSION

Research and analysis is going on the above topic. IEEE has published papers on MOSFET and IGBT degradation. Beyond device level study, there're module/circuit level experiments available also. For example, there're SiC, inverter, converter, automotive investigations of degradation and lifetime

prediction studied in many papers (see references).In some cases, there're lack of experimental set-up, and in some other cases, there're lack of new characterization techniques. So for an appropriate method or technique and satisfactory result, we've to wait having patience. Because everything needs time; trial and error method is scientific also.

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