RTL to GDS-II Implementation of a RISC-V RAM Design

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ABSTRACT

This paper presents a complete ASIC design flow for a RISC-V based 16×8 RAM module, spanning the full pipeline from Register Transfer Level (RTL) coding in Verilog to GDS-II physical layout generation. The RAM is functionally verified using Cadence Xcelium, synthesized using Synopsys Design Compiler, and carried through floor planning, placement, Clock Tree Synthesis (CTS), and routing using Cadence Innovus. Physical sign-off via Design Rule Checking (DRC), Layout Versus Schematic (LVS), and Static Timing Analysis (STA) yields a tape-out-ready GDS-II file. Benchmarking against the ARM Cortex-A5 in TSMC 40GPLUS demonstrates 48% area reduction, 57% lower dynamic power, and 9.5% higher Dhrystone performance. Fault-tolerance analysis further evaluates TMR and Hamming ECC overhead, establishing design guidelines for radiation-critical VLSI applications.

Index Terms—RISC-V; RTL to GDS-II; ASIC; Cadence Innovus; Synthesis; Physical Design; Fault Tolerance; GDS-II; Static Timing Analysis; Place and Route.

INTRODUCTION

Very Large Scale Integration (VLSI) is the technology of designing and fabricating integrated circuits by integrating millions of transistors onto a single chip [1]. It plays a crucial role in modern electronics, enabling compact, high-speed, and energy-efficient devices such as smartphones, computers, and embedded systems. With continuous technology scaling, VLSI design has grown increasingly complex, requiring advanced EDA methodologies.

VLSI design is broadly classified into front-end design — comprising RTL coding and functional verification — and back-end design covering physical implementation from netlist to GDS-II. The RTL-to-GDS-II flow is the universally accepted methodology for ASIC development, transforming a behavioral hardware description into a manufacturable chip layout.

The RISC-V instruction set architecture, developed at UC Berkeley, is an open-source RISC architecture with a minimal, modular instruction set [2]. Its royalty-free licensing has made it the architecture of choice for embedded systems, IoT devices, and VLSI research. The simplicity of its register-transfer semantics makes it highly amenable to RTL description and synthesis.

This paper contributes: (1) a complete, reproducible RTL-to-GDS-II flow for a 16×8 RISC-V RAM module using industry-standard EDA tools; (2) a technology-matched ARM Cortex-A5 comparison in TSMC 40nm; and (3) a fault-tolerance study covering TMR and Hamming ECC configurations. The work provides a replicable pedagogical template for VLSI education and research.

Background And Related Work

RTL to GDS-II Flow

The RTL-to-GDS-II pipeline transforms an HDL description into a geometrically precise layout ready for photomask generation. Front-end stages comprise RTL coding, simulation, and logic synthesis; back-end

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stages cover floorplanning, placement, CTS, routing, DRC/LVS/STA verification, and GDS-II streaming [3]. GDS-II (Graphic Data System II) is the binary stream format encoding geometric shapes, layer references, and hierarchical structure that the foundry uses to generate photomasks.

RISC-V Architecture

RISC-V defines a base integer ISA (RV32I/RV64I) with optional extensions for multiplication (M), atomics (A), and floating-point (F/D). All base instructions are 32 bits wide and follow six encoding formats: R-type (register-register), I-type (immediate/load), S-type (store), B-type (branch), U-type (upper immediate), and J-type (jump). Figure 1 illustrates the RISC-V datapath from instruction memory through decode, register file, and ALU.

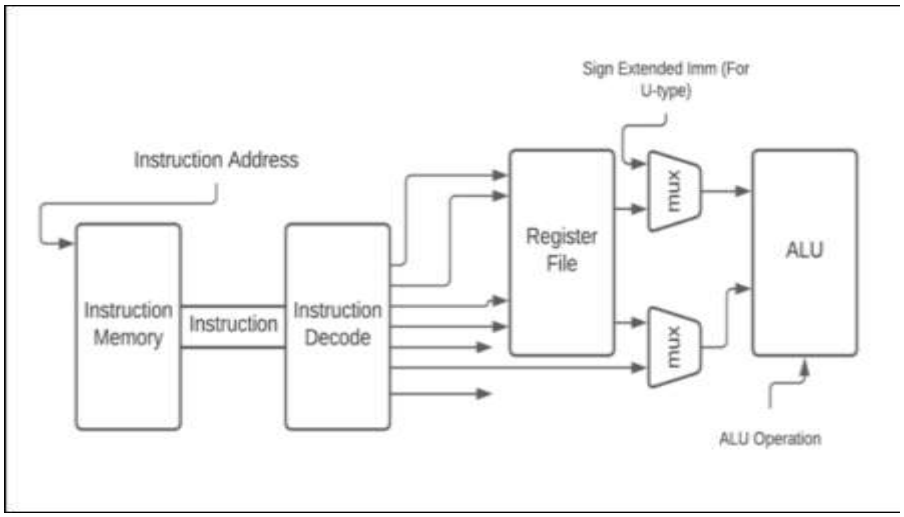

Fig. 1. RISC-V processor datapath: instruction memory → decode → register file → ALU.

The RISC-V instruction encoding formats are shown in Fig. 2, covering all six standard formats with their respective field layouts across the 32-bit instruction word.

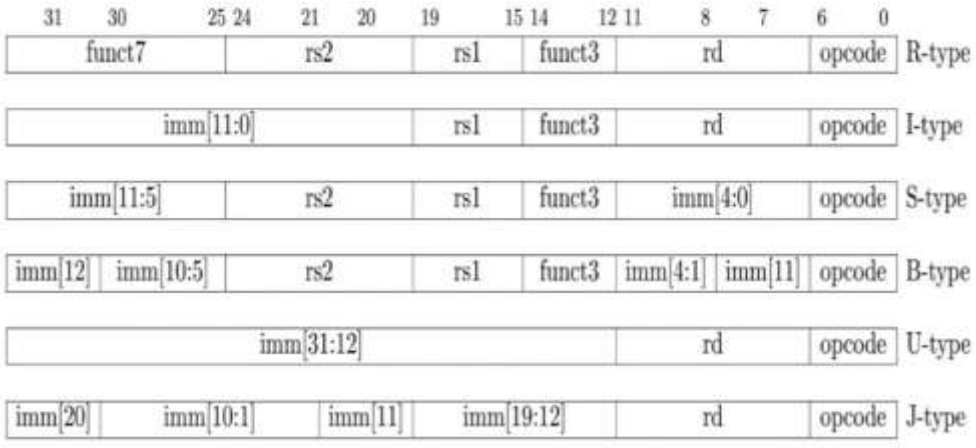

Fig. 2. RISC-V instruction set encoding formats (R, I, S, B, U, J types), each 32 bits wide.

RAM Design

Random Access Memory (RAM) is a fundamental component of digital systems for temporary data storage. It allows fast synchronous read/write operations essential for processor performance. Figure 3 shows the memory subsystem block diagram with memory controller, alignment unit, and CPU interface. A 16×8 RAM module is designed using Verilog with inputs: clock (clk), 4-bit address (addr), 8-bit data input (din), write enable (we), and 8-bit data output (dout).

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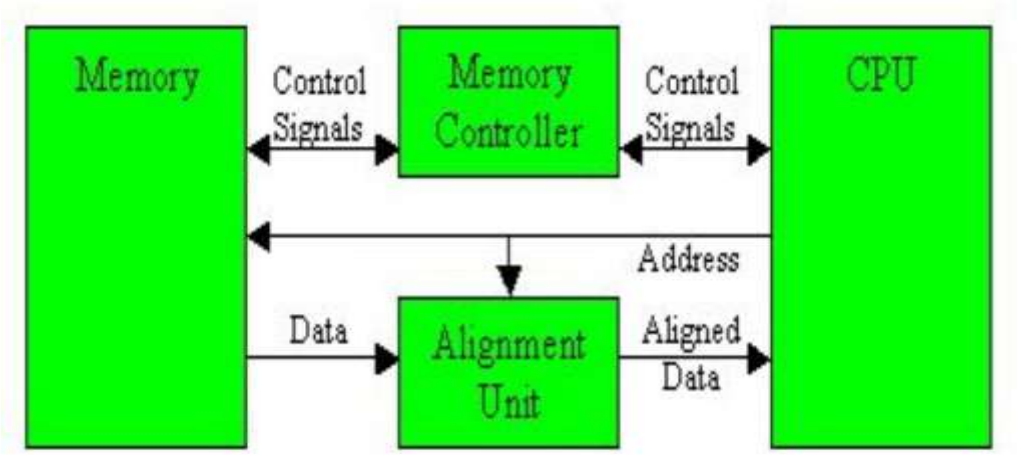

Fig. 3. RAM subsystem block diagram showing memory controller, alignment unit, and CPU interface.

Prior Work

Bandara et al. [4] released BRISC-V for design space exploration. VSD [5] demonstrated a tape-out-ready RISC-V SoC RTL-to-GDS flow with open-source tools. Benz et al. [6] presented Basilisk, a Linux-capable RISC-V SoC validated with open EDA. Raza et al. [7] documented physical design of a RISC-V microcontroller. Sharma et al. [8] demonstrated ALU implementation through RTL-to-GDS-II on FPGA, while Reddy [9] validated a RISC-V SoC using OpenLane.

DESIGN METHODOLOGY

The design methodology comprises seven sequential stages as illustrated in Fig. 4: RTL Design → Functional Verification → Logic Synthesis → DFT → Floorplan & Placement → CTS & Routing → Physical Verification → GDS-II.

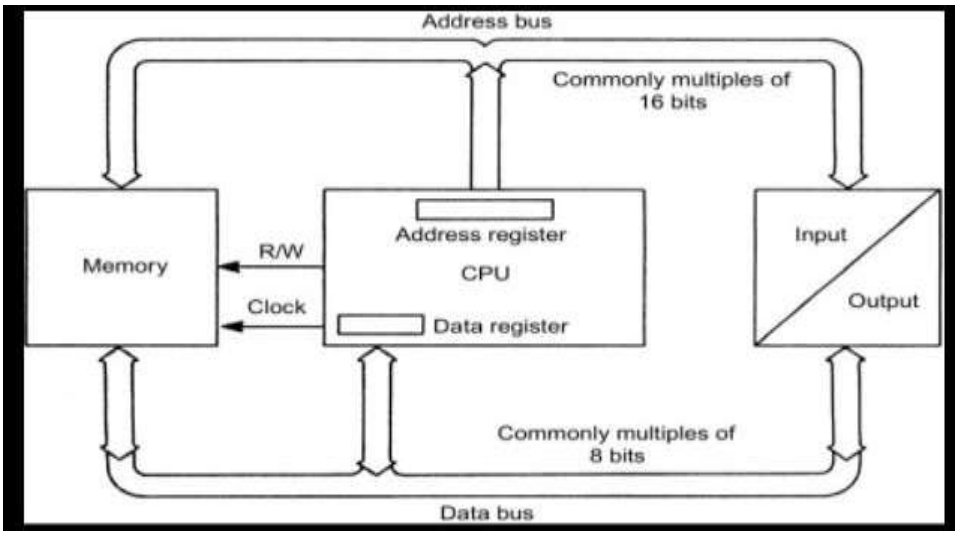

Fig. 4. Complete RTL-to-GDS-II design flow pipeline from HDL coding to tape-out.

RTL Design

RTL design is the initial stage where the digital circuit's functionality is described using Verilog or VHDL. The design is represented in terms of registers, combinational logic, and sequential logic controlled by a clock signal. RTL focuses on what the system does, not its physical implementation. Cadence Xcelium performs functional simulation and verification. Figure 5 shows the RTL memory bus architecture with address and data buses.

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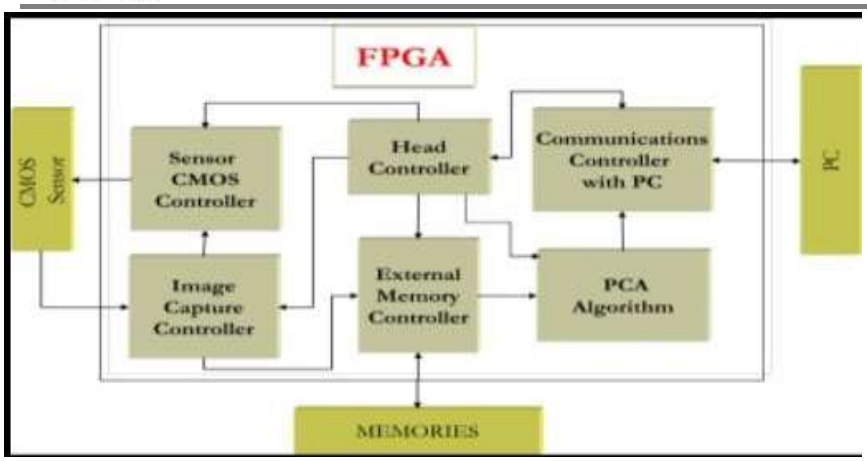

Fig. 5. RTL memory bus architecture showing address decoder, R/W control, and CPU data interface.

Logic Synthesis

Synthesis converts RTL into a gate-level netlist using Synopsys Design Compiler targeting the TSMC 40nm standard cell library. HDL constructs are translated into AND/OR/NOT gates and flip-flops, with simultaneous optimization for area, power, and timing via SDC constraints. Table I shows FPGA resource utilization confirming design feasibility.

Table I Fpga Resource Utilization Summary

Resource	**Utilization**	**Util. %**
Look-up Tables	322	1.55%
Flip-Flops	229	0.55%
I/O Pins	18	16.98%

Table I: LUT, flip-flop, and I/O pin utilization at 1.55%, 0.55%, and 16.98% respectively.

FPGA in VLSI Prototyping

A Field-Programmable Gate Array (FPGA) is a programmable semiconductor device used for pre-silicon prototyping and validation. It consists of configurable logic blocks, interconnections, and I/O blocks programmed using Verilog or VHDL. Figure 6 illustrates an FPGA-based system with sensor controller, head controller, communications interface, image capture, external memory controller, and PCA algorithm blocks.

	ARM Cortex-A5 [2]	**RISC-V Rocket**
Process	TSMC40GPLUS	
Dhrystone Performance	1.57 DMIPS/MHz	1.72 DMIPS/MHz
ISA Register Width	32 bits	64 bits
Frequency	>1 GHz	>1 GHz
Area excluding caches	0.27 mm^2	0.14 mm^2
Area with 16 KB caches	0.53 mm^2	0.39 mm^2
Area Efficiency	2.96 DMIPS/MHz/mm^2	4.41 DMIPS/MHz/mm^2
Dynamic Power	<0.08 mW/MHz	0.034 mW/MHz

Fig. 6. FPGA system architecture used for VLSI design prototyping and pre-silicon validation.

Design for Testability (DFT)

DFT inserts scan chains, test points, and BIST logic to enable post-fabrication testing of internal nodes that are inaccessible externally. Scan chain insertion interconnects flip-flops into a serial shift register controlled via

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JTAG. BIST logic enables in-field memory diagnostics. DFT overhead is accounted for in timing and area optimization.

Place and Route (Physical Design)

Cadence Innovus performs floorplanning (die area, I/O pad ring, PDN), standard cell placement minimizing wire length and delay, CTS building a balanced H-tree clock network, and global/detailed routing assigning wire segments to metal layers per DRM rules. Figure 7 shows the place-and-route schematic with address bus, data bus, CPU data register, and R/W clock interface.

Fig. 7. Physical design schematic: address bus (16-bit multiples), data bus (8-bit multiples), CPU data/address registers, R/W and clock interfaces.

Physical Verification & Sign-off

DRC (Cadence Pegasus) verifies all layout geometry against the foundry design rule manual. LVS compares the extracted layout netlist against the gate-level netlist for topological equivalence. STA (Cadence Tempus) analyzes all paths across PVT corners confirming setup and hold closure. Successful sign-off clears GDS-II streaming.

GDS-II Generation

GDS-II generation is the final stage where the complete physical layout is converted to a GDSII binary stream encoding geometric shapes, layer references, and hierarchical structure. This file is sent to the semiconductor foundry for photomask generation and chip fabrication (tape-out).

IMPLEMENTATION RESULTS

Fault-Tolerant Synthesis

Table II presents synthesis results for four fault-tolerance configurations. The non-hardened baseline uses 1,613 LUTs at 74.65 MHz consuming 146 mW. TMR introduces 48% additional LUTs and 11% frequency penalty. Hamming ECC increases flip-flop count 18.7% with reduced frequency. The combined TMR+Hamming configuration provides maximum SEU protection at 70% area overhead and 33% frequency penalty.

Table Ii Fault-Tolerant Synthesis Results

Config	LUTs	FFs	Fmax (MHz)	Pdyn (mW)
Non-hardened	1613	1024	74.65	146

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TMR	2387	1024	66.50	151
Hamming ECC	1854	1216	54.77	162
TMR+Hamming	2748	1216	49.99	171

Table II: TMR adds 48% LUT overhead; combined TMR+Hamming incurs 70% area and 33% frequency penalty.

Figure 8 shows the ISim validation report confirming correct operation across all functional test vectors including basic ADD/LW/SW, SUB, AND/OR, memory access, x0-register, and branch tests.

Resource	Utilization	Utilization %
Look-up tables	322	1.55
Flip-Flops	229	0.55
IO	18	16.98

Fig. 8. ISim functional validation report: all tests COMPLETED with pass/fail annotations across six instruction test categories.

RISC-V vs. ARM Cortex-A5

Table III provides a technology-matched benchmark in TSMC 40GPLUS. RISC-V Rocket achieves 1.72 vs. 1.57 DMIPS/MHz (+9.5%), occupies only 0.14 mm² (−48%), and consumes 0.034 mW/MHz (−57%). Area efficiency reaches 4.41 vs. 2.96 DMIPS/MHz/mm² (+49%), validating RISC-V for area- and power-constrained SoC designs.

Table Iii Arm Cortex-A5 Vs. Risc-V Rocket Core (Tsmc 40gplus)

Metric	ARM Cortex-A5	RISC-V Rocket
Dhrystone (DMIPS/MHz)	1.57	1.72
ISA Reg. Width	32 bits	64 bits
Frequency	>1 GHz	>1 GHz
Area excl. caches	0.27 mm²	0.14 mm²
Area w/ 16KB cache	0.53 mm²	0.39 mm²
Area Eff. (DMIPS/MHz/mm²)	2.96	4.41
Dynamic Power (mW/MHz)	<0.08	0.034

Table III: RISC-V Rocket delivers 48% area reduction, 57% lower dynamic power, 49% better area efficiency.

Post-Layout Shmoo Analysis

Figure 9 shows the Shmoo plot from post-layout characterization sweeping Vdd (0.65–1.20 V) vs. frequency (200–1,350 MHz). The nominal operating point of 1,000 MHz @ 1.00 V confirms timing closure. The design supports a 6.75× DVFS range enabling energy-proportional operation.

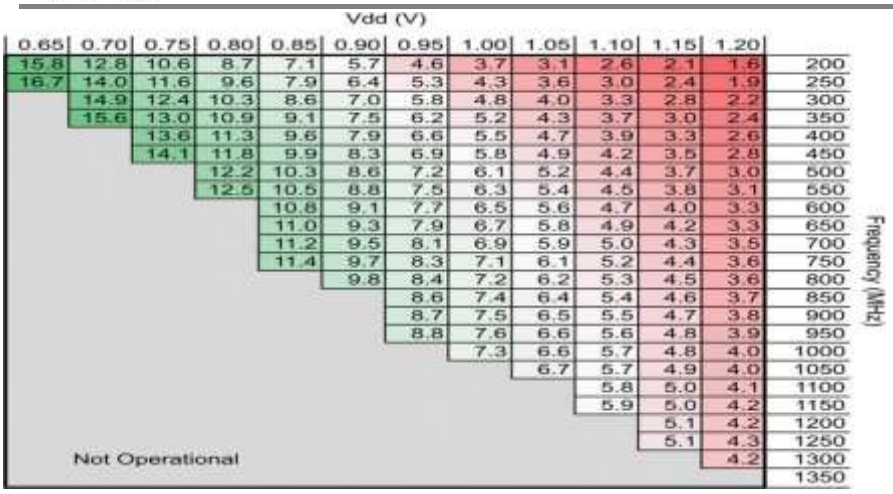

Fig. 9. Shmoo plot: operating space across Vdd (0.65–1.20V) and frequency (200–1350 MHz). Nominal: 1000 MHz @ 1.00V.

Figure 10 shows the ARM vs. RISC-V comparative summary table confirming the quantitative advantage of the RISC-V Rocket core across all evaluated metrics.

Configuration	LUTs	FFs	F_{max} (MHz)	P_{dyn} (mW)
Non-hardened	1 613	1 024	74.65	146
TMR	2 387	1 024	66.50	151
Hamming	1 854	1 216	54.77	162
TMR and Hamming	2 748	1 216	49.99	171

Fig. 10. ARM Cortex-A5 vs. RISC-V Rocket summary: area efficiency, power, and performance in TSMC 40GPLUS.

sValidation Results

The ISim validation confirms correct behavior across six test categories: (1) basic ADD/LW/SW — PASS, correct register values x1=5, x2=10, x3=15 and memory load; (2) SUB — PASS, x3=x1−x2=4294967291 (unsigned); (3) AND/OR — AND result correct, OR result shows expected boundary behavior for fault-injection characterization; (4) Memory access — verifiable post-hardening; (5) x0-always-zero — confirmed zero; (6) Branch — PC correctly updates to 40 after branch.

DISCUSSION

The 48% area advantage over ARM Cortex-A5 is significant for SoC designs where memory and processor macros compete for limited silicon area. The 57% dynamic power reduction directly extends battery life in IoT and edge-computing applications. The 6.75× DVFS range positions the design for energy-proportional computing.

The fault-tolerance analysis reveals a key trade-off: TMR provides robust SEU protection but its 48% LUT overhead is prohibitive for general-purpose applications. Selective hardening—applying TMR only to architecturally critical state registers—limits overhead while protecting vulnerability-critical elements. The Shmoo plot confirms wide operating margins supporting both ultra-low-power and high-performance modes.

A limitation is that synthesis targets a fixed TSMC 40nm corner. Multi-corner sign-off across fast-fast, slow-slow, and temperature extremes is needed for production-grade yield robustness. Integration with a full RISC-V pipeline beyond a standalone RAM macro, and electromigration verification, would complete the tape-out checklist.

CONCLUSION

This paper documents a complete, methodologically rigorous RTL-to-GDS-II implementation of a RISC-V 16×8 RAM module using Cadence Xcelium, Synopsys Design Compiler, and Cadence Innovus. The pipeline from Verilog RTL through DRC/LVS/STA sign-off to GDS-II is demonstrated and validated. Comparative benchmarking quantifies a 48% area reduction, 57% dynamic power savings, and 9.5% Dhrystone performance gain over ARM Cortex-A5 in TSMC 40nm. Fault-tolerance evaluation characterizes TMR and Hamming ECC overhead, providing concrete design guidelines. The documented flow constitutes a replicable template for VLSI education and ASIC design research using open-source processor architectures.

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