Switching Reduction in a Symmetrical Cascaded Diode-Clamped Multilevel Inverter (SCDC MLI)

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ABSTRACT

Multilevel inverters (MLIs) are widely used in high-power applications because they offer lower harmonic distortion than conventional inverters. The three common MLI topologies are cascaded H-bridge, diode-clamped, and flying-capacitor inverters. However, conventional topologies require a large number of switching devices to achieve higher voltage levels, resulting in increased switching losses, hardware size, weight, cost, and control complexity. This project aims to simulate a symmetrical cascaded switching diode (SCSD) multilevel inverter topology, which uses fewer switching devices to reduce switching losses and simplify the circuit design. Single-phase and three-phase seven-level SCSD MLI topologies will be designed and simulated using MATLAB/Simulink. The simulation results will be analysed based on voltage total harmonic distortion (THDV) and current total harmonic distortion (THDI) under several of loads. Two switching techniques, namely triangular-wave switching and sinusoidal pulse-width modulation (SPWM), will be evaluated for both single-phase and three-phase configurations. The results show that the RL load produces the lowest (THDI) compared with the R and RC loads. For the single-phase configuration, the (THDI) values are 6.98% for triangular-wave switching and 5.82% for SPWM. For the three-phase configuration, the corresponding values are 0.89% and 0.88%, respectively. The (THDV) values for the four configurations are 25.47%, 47.90%, 11.91%, and 29.18%, respectively. Compared with conventional MLI topologies, which generally require more switching components, the proposed SCSD topology uses only seven switching devices to generate a seven-level output voltage. This reduction in the number of switching devices has the potential to reduce switching losses, hardware complexity, size, and cost.

Keywords: Multilevel Inverter, Symmetrical Cascaded Diode Claimed, Total Harmonic Distortion, Pulse Width Modulation, MATLAB/Simulink,

INTRODUCTION

Inverters are widely used in various industries to convert direct current (DC) into alternating current (AC). Some industrial equipment requires high power to operate, while other equipment operates at medium or low power levels. Therefore, an appropriate power conversion system is essential to ensure efficient and reliable operation [1-2]. Traditionally, inverters were mainly used to supply AC power to loads when the utility grid was unavailable. Nowadays, multilevel inverters (MLIs) have gained significant attention in industrial applications due to their improved output voltage quality and reduced harmonic distortion. These advantages have encouraged the development of various MLI topologies [3-7]. The main purpose of a multilevel inverter is to convert DC power into AC power by switching between different DC voltage levels to produce a stepped output voltage waveform that closely approximates a sinusoidal waveform. This approach can reduce harmonic distortion and improve the overall performance of the power conversion system.

Since the development of multilevel inverters in the 1970s, various topologies have been introduced to improve inverter performance. Compared with conventional inverters, multilevel inverters offer several advantages, including higher voltage capability, improved output voltage quality, and reduced total harmonic distortion (THD). A multilevel inverter consists of multiple power switching devices that are controlled to generate stepped

output voltage levels. These voltage levels produce an output waveform that closely approximates a sinusoidal waveform, improving power quality and reducing harmonic distortion [8-9].

The three main topologies of multilevel inverters (MLIs) are the cascaded H-bridge, flying-capacitor, and diode-clamped topologies. Various switching techniques can be used to control these inverters, including bipolar sinusoidal pulse-width modulation (SPWM), unipolar SPWM, space vector modulation (SVM), parti-

cle swarm optimisation (PSO), and selective harmonic elimination (SHE). This project focuses on comparing triangular-carrier switching and sinusoidal pulse-width modulation (SPWM) techniques for a symmetrical cascaded switched-diode (SCSD) multilevel inverter. The performance of the SCSD topology will be evaluated based on the total harmonic distortion of voltage (THDV) and current (THDI), considering different modulation indices and both single-phase and three-phase inverter configurations. The proposed SCSD topology aims to reduce the number of switching devices, switching losses, installation space, and overall system cost. MATLAB/Simulink simulations will be conducted to evaluate the operation and performance of the proposed multilevel inverter under different operating conditions [9].

This study investigates the performance of four Symmetrical Cascaded Switched Diode (SCSD) multilevel inverter (MLI) configurations: single-phase triangular SCSD, single-phase SPWM SCSD, three-phase triangular SCSD, and three-phase SPWM SCSD. The main objective is to evaluate and compare their total harmonic distortion (THD) performance under different load conditions, namely resistive (R), resistive-inductive (RL), and resistive-capacitive (RC) loads. This study involves modeling and simulation using MATLAB/Simulink. All four inverter configurations are developed and simulated to produce a seven-level output voltage. Their performance is evaluated under the specified load conditions by measuring and analyzing the output voltage and current THD. The amplitude modulation index (Ma) is varied from 0 to 1 to investigate its effect on the harmonic performance of the single-phase and three-phase SPWM SCSD multilevel inverters. The SCSD multilevel inverter topology is considered due to its potential to reduce the number of power switches and associated power losses compared with conventional multilevel inverter configurations. The simulation results are analyzed and compared to determine the effects of inverter configuration, modulation technique, load type, and amplitude modulation index on THD performance.

LITERATURE REVIEW

The symmetrical multilevel diode inverter is designed to reduce the number of power switches required for medium-voltage applications. Several cascaded units are used to generate a stepped output voltage waveform with lower total harmonic distortion (THD) [14]. The conventional and proposed topologies are compared based on the number of isolated-gate bipolar transistors (IGBTs), power diodes, and overall power losses. The stepped output voltage waveform of a multilevel inverter provides a closer approximation to a sinusoidal waveform than that of a conventional two-level inverter. In a symmetrical topology, all DC voltage sources have equal magnitudes, whereas an asymmetrical topology uses DC sources with different voltage magnitudes. The SCSD topology consists of three isolated DC voltage sources and seven IGBTs, enabling it to generate up to seven voltage levels, including zero and both positive and negative levels. Figure 1 illustrates the single-phase Symmetrical Cascaded Switched-Diode (SCSD) multilevel inverter topology.

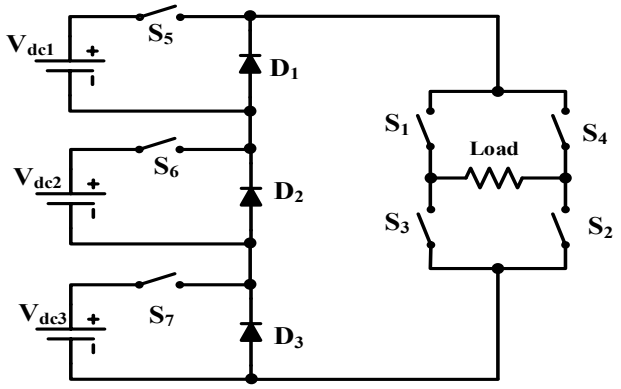


Figure 1: Single phase 7-level of Symmetrical Cascaded Switched-Diode

In the Symmetrical Cascaded Switched-Diode (SCSD) topology, the number of switches required can be determined using Equation (1). For example, a seven-level output voltage requires seven switches to operate. In this equation, (N) represents the number of DC voltage sources. Meanwhile, the number of output voltage levels can be calculated using Equation (2), where (n) represents the number of cascaded circuits.

$$No.\ of\ Switch = 2N + 1 \quad (1)$$

Where N = Number of DC Voltage

$$Output\ level = 2n + 3 \quad (2)$$

Where n = number of cascaded circuit.

The symmetrical configuration offers a more modular structure and simpler control strategy than the asymmetrical configuration. However, increasing the number of output voltage levels requires more independent DC voltage sources and power semiconductor switches, resulting in a larger multilevel inverter (MLI) size and increased system complexity [13]. Table 1 presents the switching sequence for the 7-level symmetrical cascaded switched-diode topology, which generates the PWM switching signals and output voltage waveforms shown in Figures 2(a) and 2(b), respectively.

Table 1: Switching sequence for 7-level symmetrical cascaded switched diode topology

Voltage level	Switching sequences						
	S_1	S_2	S_3	S_4	S_5	S_6	S_7
0Vdc	1	1	0	0	0	0	0
+Vdc	1	1	0	0	1	0	0
+2Vdc	1	1	0	0	1	1	0
+3Vdc	1	1	0	0	1	1	1
+3Vdc	1	1	0	0	1	1	1
+2Vdc	1	1	0	0	1	1	0
+Vdc	1	1	0	0	1	0	0
0Vdc	1	1	0	0	0	0	0
0Vdc	0	0	1	1	0	0	0
-Vdc	0	0	1	1	1	0	0
-2Vdc	0	0	1	1	1	1	0
-3Vdc	0	0	1	1	1	1	1
-3Vdc	0	0	1	1	1	1	1
-2Vdc	0	0	1	1	1	1	0
-Vdc	0	0	1	1	1	0	0
0Vdc	0	0	1	1	0	0	0

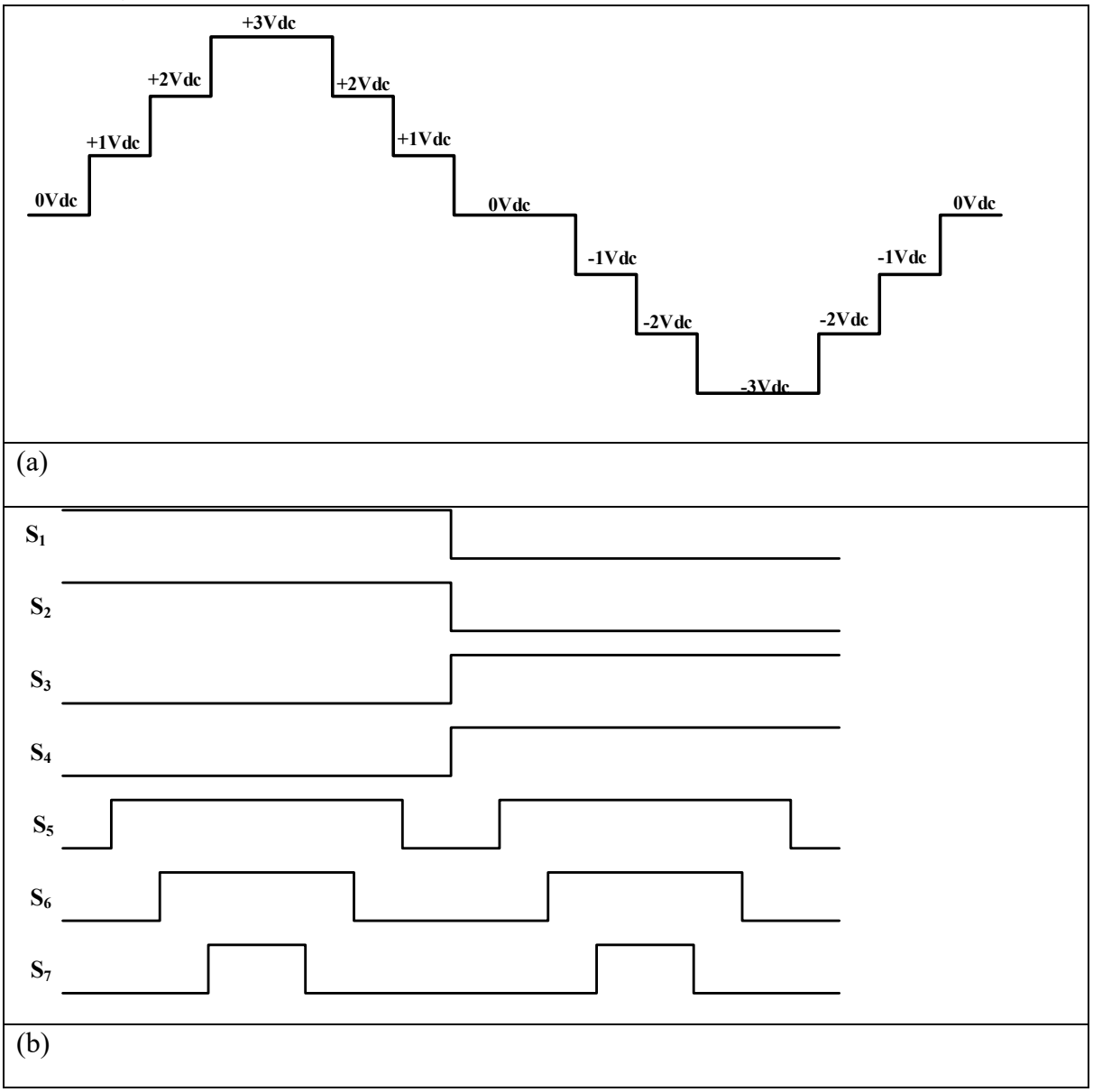


Figure 2: (a) PWM switching signal (b)7-level output waveform (b)

The comparison in Table 2 presents the number of power switches, capacitors, and diodes required by conventional multilevel inverter (MLI) topologies and the symmetrical cascaded switched-diode (SCSD) topology to generate a seven-level output voltage. The SCSD topology requires only seven power switches and three diodes, reducing the number of controllable switches compared with the conventional cascaded H-bridge (CHB), diode-clamped (DC), and flying-capacitor (FC) topologies. Furthermore, SCSD does not require additional capacitors in the configuration considered, which may simplify its circuit structure and reduce implementation complexity. The SCSD topology may also offer improved total harmonic distortion (THD) performance and suitability for high-voltage applications.

Table 2: Comparison of the number of power switches, capacitors, and diodes between conventional MLI and SCSD topologies for seven-level output voltage

Multilevel inverter topology	Numbers of switches	Numbers of capacitor	Numbers of diode
Cascaded H-bridge (CHB)	12	-	-
Clamped diode (CD)	12	-	10
Flying capacitor (FC)	12	21	-
Symmetrical cascaded switched diode (SCSD)	7	-	3

METHODOLOGY

The three-phase Sinusoidal Pulse Width Modulation (SPWM) Symmetrical Cascaded Switched-Diode (SCSD) multilevel inverter is designed and simulated using MATLAB/Simulink, as shown in Figure 3. The model consists of five main components: the switching signal generator, SPWM generator, DC voltage source (Vdc), SCSD inverter circuit, and load block. The switching signal generator controls the seven IGBT switches (S1–S7) according to predefined switching states to produce a seven-level output voltage. The SPWM block generates sinusoidal pulse signals for switches S5, S6, and S7, while switches S1–S4 operate according to their predefined switching patterns. The Vdc block supplies the required input voltage, while the SCSD inverter circuit uses seven IGBTs and three diodes to generate the multilevel output waveform. The load block is used to evaluate inverter performance with resistive (R), resistive-inductive (RL), and resistive-capacitive (RC) loads. To develop the three-phase configuration, two additional single-phase inverter sections are incorporated, with reference signals shifted by 120 degrees. Finally, the simulation captures the phase currents, phase voltages, and line-to-line voltages to evaluate output waveform quality and total harmonic distortion (THD)

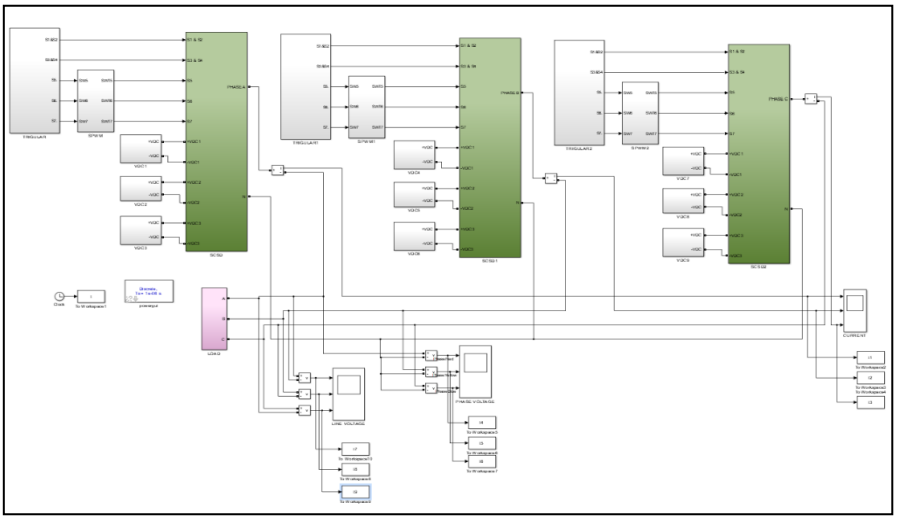


Figure 3: Simulink block for Three-phase SPWM SCSD Multilevel Inverter

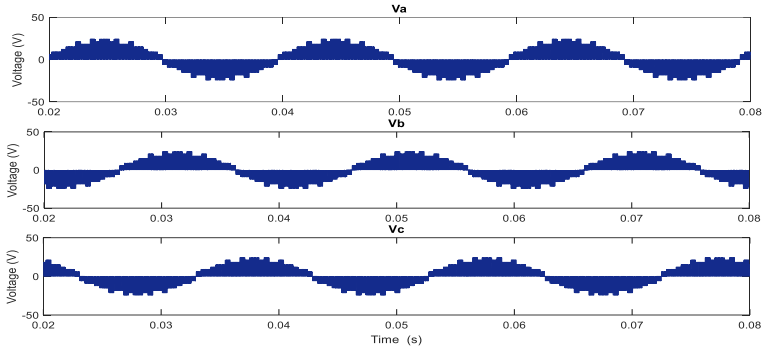
Table 3 shows the simulation parameters used to model the three-phase SPWM SCSD multilevel inverter in MATLAB/Simulink. The parameters include the DC input voltage, R, RL, and RC load values, diode resistance, fundamental frequency, and carrier frequency. The fundamental and carrier amplitudes are set to 1 V, while the carrier frequency is set to 10 kHz to generate the PWM switching signals. The phase delays of 0°, 120°, and 240° are used to produce the three-phase output. These parameters are applied to evaluate the inverter's output voltage, phase current, and total harmonic distortion (THD) under different load conditions.

Table 3: Parameter of three phase SPWM Symmetrical Cascaded Switched Diode MLI simulation

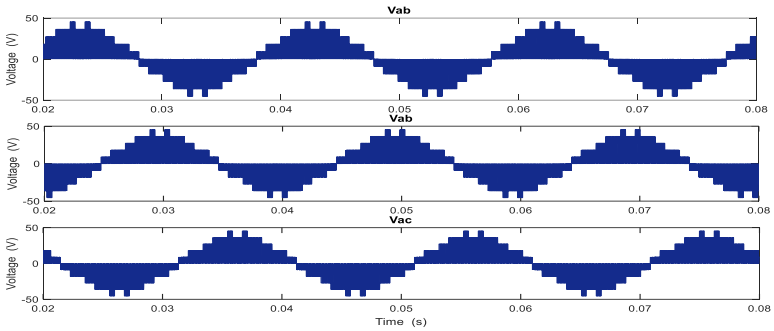
Parameter	**Value**
Voltage source for each input	100 V
Resistive load	100 Ω
Capacitive load	1.5 mF
Inductive load	5 H
Resistance for each diode	0.001 Ω
Fundamental frequency	50 Hz
Fundamental amplitude	1 V
Carrier frequency	10 kHz
Carrier amplitude	1 V
Phase delay	Phase A: 0°, Phase B: 120°, Phase C: 240°

RESULTS AND DISCUSSION

Figures 4(a) and 4(b) show the phase and line voltages, respectively, of the three-phase SPWM SCSD MLI under R, RL, and RC load conditions at a modulation index of 1. The waveforms demonstrate the inverter's ability to generate multilevel output voltages. Figures 5(a), 5(b), and 5(c) present the three-phase line currents for the R, RL, and RC loads, respectively. The R load produces current approximately in phase with the voltage, while the RL load results in smoother, lagging current due to the inductance. In contrast, the RC load typically produces leading current. These differences highlight the influence of load characteristics on the inverter's output performance and harmonic distortion.

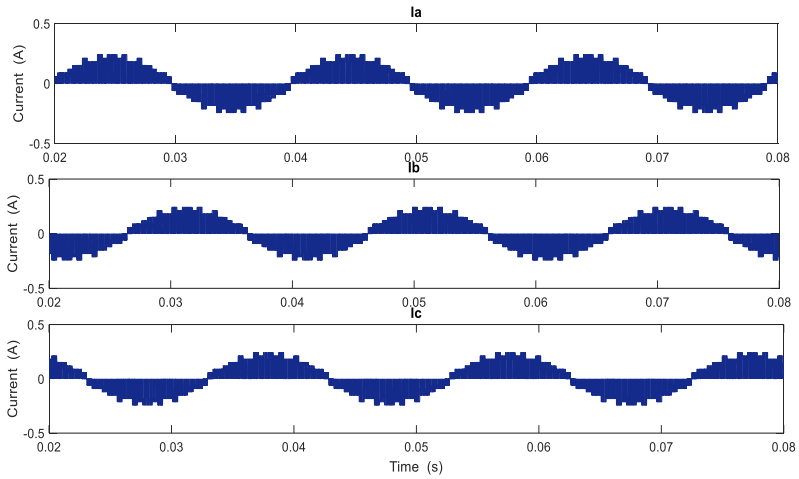


(a)

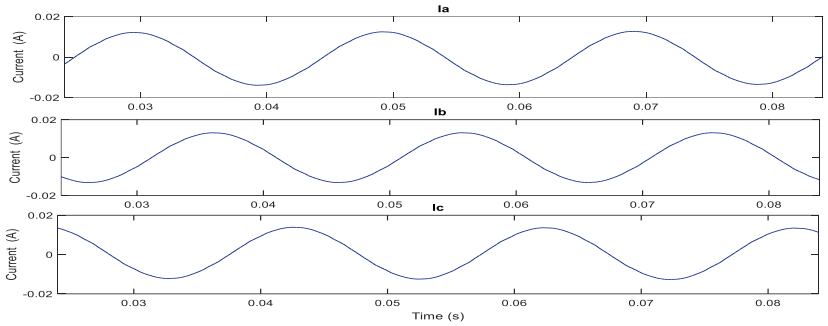


(b)

Figure 4: (a) Phase Voltage waveform for three phase SPWM SCSD MLI topology for R, RL and RC load (b) Phase Voltage waveform for three phase SPWM SCSD MLI topology for R, RL and RC load



(a)



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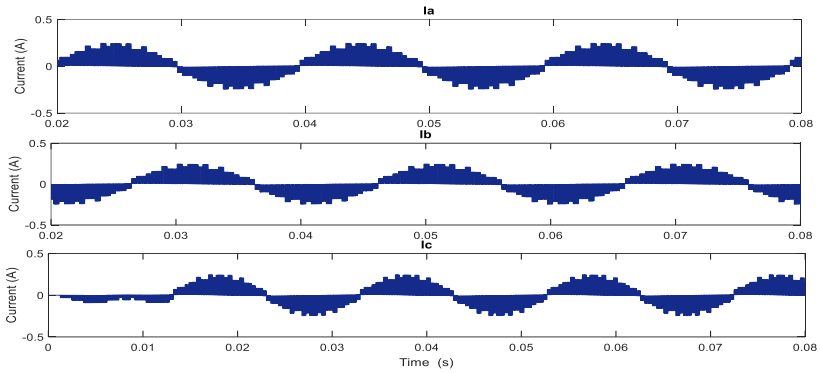
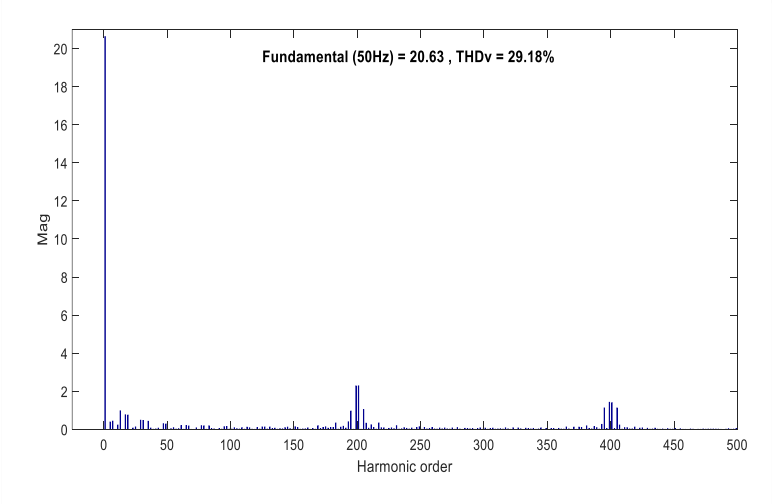


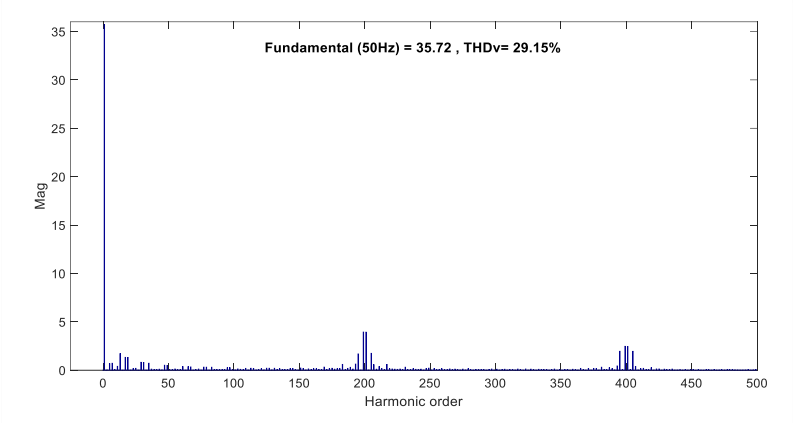
(c)

Figure 5: (a) Line current waveform for three phase SPWM SCSD MLI topology for R load (b) Line current waveform for three phase SPWM SCSD MLI topology for RL load (c) Line current waveform for three phase SPWM SCSD MLI topology for RC load

Figures 6(a) and 6(b) show the THDv of the phase and line voltages, respectively, for the three-phase SPWM SCSD MLI under R, RL, and RC load conditions at a modulation index of 1. The simulation results indicate relatively similar THDv values, demonstrating consistent voltage harmonic characteristics across the different loads. Figures 7(a), 7(b), and 7(c) present the THDi of the line currents for R, RL, and RC loads, respectively. The RL load exhibits lower THDi due to the inductance, which reduces current ripple and high-frequency harmonics. In contrast, the R and RC loads produce different harmonic responses depending on their electrical characteristics. Table 4 summarises the THDv and THDi results for all three load conditions at a modulation index of 1.

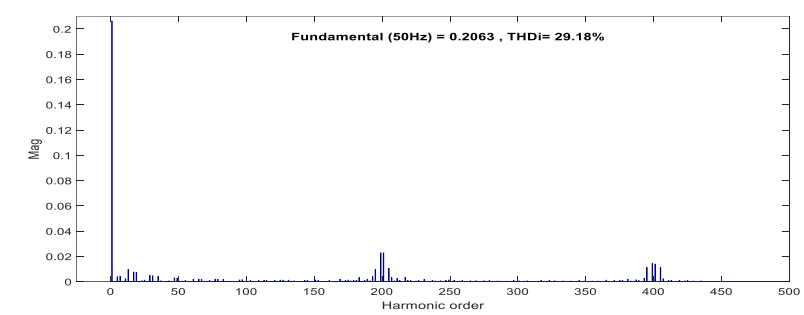


(a)

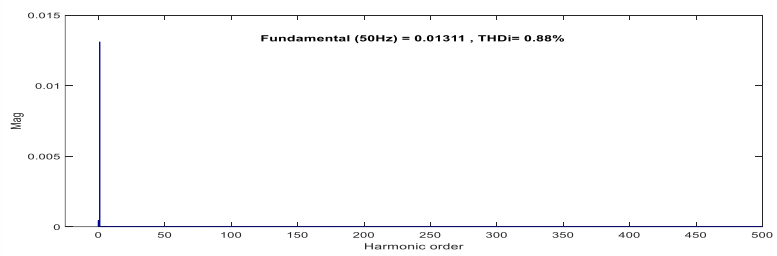


(b)

Figure 6: (a) THD_V for phase voltage in three phase SPWM SCSD topology for R, RL and RC load (b) THD_V for line voltage in three phase SPWM SCSD topology for R, RL and RC load



(a)



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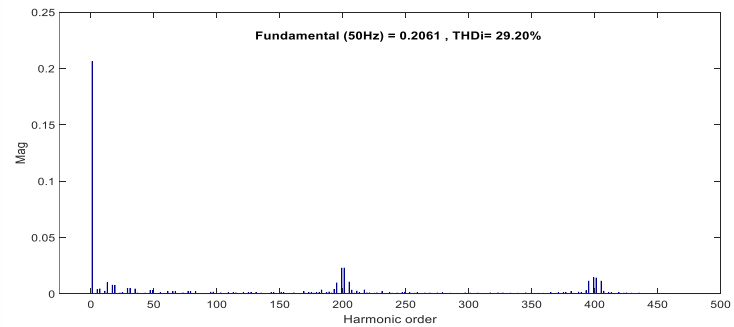

(c)

Figure 7: (a) THD_i for line current in three phase SPWM SCSD topology for R load (b) THD_i for line current in three phase SPWM SCSD topology for RL load (c) THD_i for line current in three phase SPWM SCSD topology for RC load

Table 4 : THD Results of Three-Phase SPWM SCSD Multilevel Inverter for $M_a = 1$

Load Type	THD Phase Voltage (%)	THD Line Current (%)	THD Line Voltage (%)
R load	29.18	29.18	29.15
RL load	29.18	0.88	29.15
RC load	29.18	29.2	29.15

Figure 8 illustrates the variation of current total harmonic distortion (THD_i) with different amplitude modulation indices for the three-phase SPWM SCSD topology. It can be observed that THD_i decreases as the amplitude modulation index increases. At a lower modulation index, the fundamental component of the output current is relatively small compared to its harmonic components, resulting in higher THD current. As the modulation index increases, the fundamental output voltage increases, leading to a higher fundamental current component and a reduction in the relative contribution of harmonic currents.

Furthermore, the reduction in current THD indicates an improvement in the sinusoidal quality of the output current. This is important for three-phase AC applications, as lower current harmonic distortion helps to improve power quality and reduce additional losses in electrical components. Therefore, the selection of an appropriate amplitude modulation index is important to achieve better harmonic performance in the proposed three-phase SPWM SCSD topology

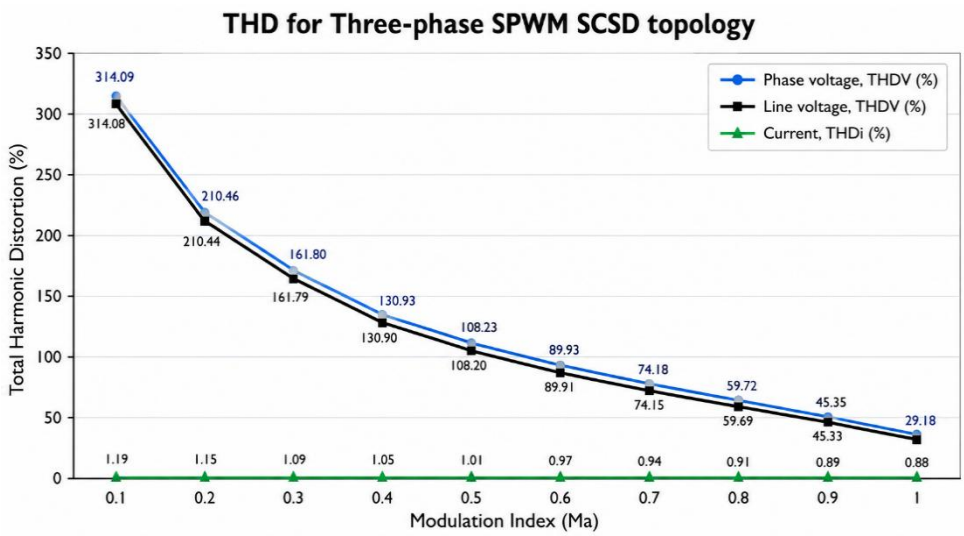

Figure 8: THD volatge and current for three-phase SPWM SCSD topology

CONCLUSION AND RECOMMENDATIONS

The simulation results demonstrate the performance of four SCSD multilevel inverter configurations: single-phase triangular carrier, single-phase sinusoidal pulse-width modulation (SPWM) carrier, three-phase triangular carrier, and three-phase SPWM carrier. The results show slight differences in the total harmonic distortion (THD) of the output voltage and current among the configurations. A comparison between the triangular and SPWM carrier techniques indicates that the carrier modulation method influences the harmonic performance of the inverter. In general, increasing the modulation index towards 1 reduces the percentage of THD, as observed in the simulation results. Furthermore, the voltage THD remains consistent across the tested configurations and load conditions, according to the results obtained. The SCSD topology also offers an advantage in reducing the number of power switching devices required to generate a multilevel output voltage. This reduction can lower component costs, simplify the circuit structure, and potentially reduce switching losses associated with IGBT operation. Compared with conventional multilevel inverter topologies that may require more switching devices and complex control strategies, the SCSD topology provides a simpler alternative for multilevel voltage generation. Therefore, the simulation study demonstrates the potential of the SCSD topology to achieve reduced

component requirements while maintaining satisfactory harmonic performance. These findings support its suitability for further investigation in multilevel inverter applications.

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Conflict of Interest Statement

The authors declare that this research was carried out without any commercial or financial relationship that could be taken as a potential conflict of interest.

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