Virtual Fabrication and Performance Development of V_{TH} and I_{OFF} in 7.3 Nm Double-Gate MOSFET

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ABSTRACT

This study presents the virtual design and baseline electrical evaluation of a 7.3 nm double-gate MOSFET (DG-MOSFET) incorporating a bilayer graphene channel, a titanium dioxide (TiO_2) high-k dielectric, and tungsten silicide (WSi_x) gates. The process structure was developed using Silvaco ATHENA, and its electrical characteristics were evaluated using Silvaco ATLAS. The device is assessed against the high-performance logic targets cited from the International Technology Roadmap for Semiconductors (ITRS), where a threshold voltage magnitude of approximately 0.23 V with a ±12.7% tolerance and an off-state leakage-current target below 100 nA/µm. The simulated threshold-voltage magnitudes are 0.2251 V for PMOS and 0.2597 V for NMOS. The corresponding reported off-state currents are 92.4 nA/µm for PMOS and 93.37 nA/µm for NMOS. The successful realization of this virtual device establishes a foundation for subsequent statistical optimization studies and provides insights into the development of highly reliable and energy-efficient nanoscale semiconductor devices.

Keywords— MOSFET, Bilayer graphene, TiO_2, WSi_x, TCAD, Leakage current, Threshold voltage.

INTRODUCTION

Continuous scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) has enabled remarkable advancements in integrated circuit technology. However, as device dimensions approach the sub-10-nm regime, severe short-channel effects (SCEs), threshold voltage instability, and excessive leakage current become critical challenges that limit device performance and reliability [1]. Conventional SiO_2/polycrystalline-silicon (poly-Si) gate structures are no longer suitable due to increased quantum tunnelling and gate leakage, resulting in significant power dissipation [2] [3].

To overcome these limitations, high-k/metal-gate (HKMG) technology has emerged as an effective solution for advanced CMOS devices [4]. Titanium dioxide (TiO_2), with its high dielectric constant and excellent thermal stability, provides improved gate control while reducing leakage current [5] [6]. In addition, tungsten silicide (WSi_x) metal gates eliminate poly-depletion effects and enable better work-function engineering, making the TiO_2/WSi_x gate stack a promising candidate for nanoscale transistor applications [7].

Recent studies have demonstrated improvements in transistor characteristics through the implementation of high-k dielectrics, metal gates, graphene-based channels, and double-gate architectures [8],[9],[10]. Nevertheless, most reported devices employ larger technology nodes or different material combinations, while limited studies have investigated the integration of a bilayer graphene channel with a TiO_2/WSi_x gate stack in a 7.3 nm double-gate MOSFET structure. Therefore, further investigation is required to evaluate the electrical characteristics of this device configuration, particularly its threshold voltage (V_{TH}) and leakage current (I_{OFF}) [11] .

Virtual fabrication and TCAD-based device simulation have been widely employed in semiconductor device research to evaluate and optimize device structures and electrical characteristics prior to physical fabrication. This simulation-based approach enables researchers to investigate device parameters and identify suitable process conditions while reducing the cost and time associated with experimental fabrication. Such virtual fabrication approaches have also been applied to nanoscale MOSFETs, where key electrical parameters such as V_{TH} and I_{OFF} are extracted and optimized against established technology targets [12] [13] [15]. Published work on bilayer-graphene MOSFET structures provides a relevant modelling reference, although its reported 22 nm device dimensions and material assumptions cannot be transferred directly to the present 7.3 nm design [16].

This work presents the virtual process design and preliminary electrical characterization of a 7.3 nm bilayer-graphene DG-MOSFET with a TiO_2 dielectric and WSi_x gates using Silvaco ATHENA and ATLAS. The reference specification is taken from the International Technology Roadmap for Semiconductors (ITRS) for high-performance specifications [17]. The cited target is approximately 0.23 V (±12.7%) for threshold voltage and below 100 nA/µm for off-state current. The study reports baseline V_{TH} and I_{OFF} values; optimization and claims of improvement are reserved until comparative simulations and the additional performance metrics have been completed [18].

Process and Device Structure

Fabrication Process

Silvaco ATHENA was employed to virtually fabricate the 7.3 nm double-gate MOSFET (DG-MOSFET) structure, while Silvaco ATLAS was used to perform device simulations and evaluate its electrical characteristics. The proposed device incorporates a bilayer graphene channel, TiO_2 as the high-k gate dielectric, and WSi_x as the metal gate electrode, with the gate electrodes positioned on opposite sides of the channel to form the DG configuration. All three materials, namely graphene, TiO_2, and WSi_x, were selected from the available material library in Silvaco ATLAS and assigned to their respective regions within the device structure. The built-in material properties available in the ATLAS material library were used for the electrical simulations.

Two transistor configurations, namely PMOS and NMOS, were considered in this study. The PMOS structure consists of an n-type silicon body with p-type source and drain regions, whereas the NMOS structure consists of a p-type silicon body with n-type source and drain regions. Both structures were developed using a conventional top-down fabrication approach, following a sequence of standard semiconductor processing steps. Selected process parameters, particularly doping concentrations and annealing temperatures, were adjusted to achieve the desired device characteristics based on the ITRS high-performance logic technology targets. The virtual fabrication process was carried out using the ATHENA module through a defined sequence of fabrication steps, commonly referred to as a process flow. Subsequently, the resulting device structures were transferred to the ATLAS module for electrical characterization, focusing particularly on threshold voltage (V_{TH}) and off-state leakage current (I_{OFF}). Table 1 and Table 2 present a summary of the design parameters and specifications for the NMOS and PMOS transistors, respectively.

Table 1. Fabrication Parameter of PMOS

Process Step	**Parameters**
N-Type Silicon	<100> orientation
Threshold Voltage Implantation	0.99×10^{11} atom/cm^2

Bilayer Graphene Deposition	Thickness = 0.001 µm (1 nm)
High-K deposition	Thickness = 0.003 µm (3 nm) of TiO_2
Metal Gate Deposition	7.3 nm length, 0.15 µm thickness of WSi_x
S/D implantation	$4.97x10^{14}$ atoms/cm^2 Boron
Aluminium Deposition	Thickness = 0.01 µm

Table 2. Fabrication Parameter of NMOS

Process Step	**Parameters**
P-Type Silicon	<100> orientation
Threshold Voltage Implantation	8.99 x 10^{11} atom/cm^2
Bilayer Graphene Deposition	Thickness = 0.001 µm (1nm)
High-K deposition	Thickness = 0.003 µm (3nm) of TiO_2
Metal Gate Deposition	7.3 nm length, 0.15 µm thickness of WSi_x
S/D implantation	$1.27x10^{18}$ atoms/cm^2 Arsenic
Aluminium Deposition	Thickness = 0.01 µm

The fabrication result for complete 7.3 nm DG-MOSFET transistor in Silvaco ATHENA are shown in Figure I. The two WSi_x electrodes are intended to provide opposing gate control across the bilayer-graphene channel, with TiO_2 separating each gate from the channel. Hence, the doping profile of the 7.3 nm DG-MOSFET transistor is shown in Figure 2. Figure 3 portrays the designed PMOS device's I_{DS}-V_{DS} characteristics while Figure 4 portrays the PMOS devices I_{DS}-V_{GS} characteristics.

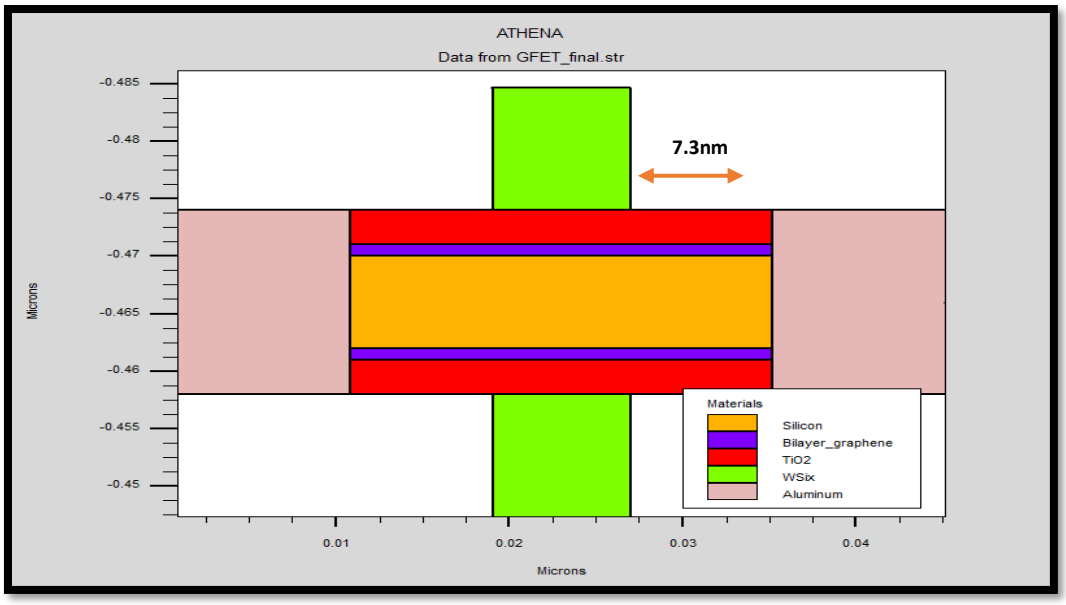


Figure 1. The complete 7.3 nm DG-MOSFET virtual transistor

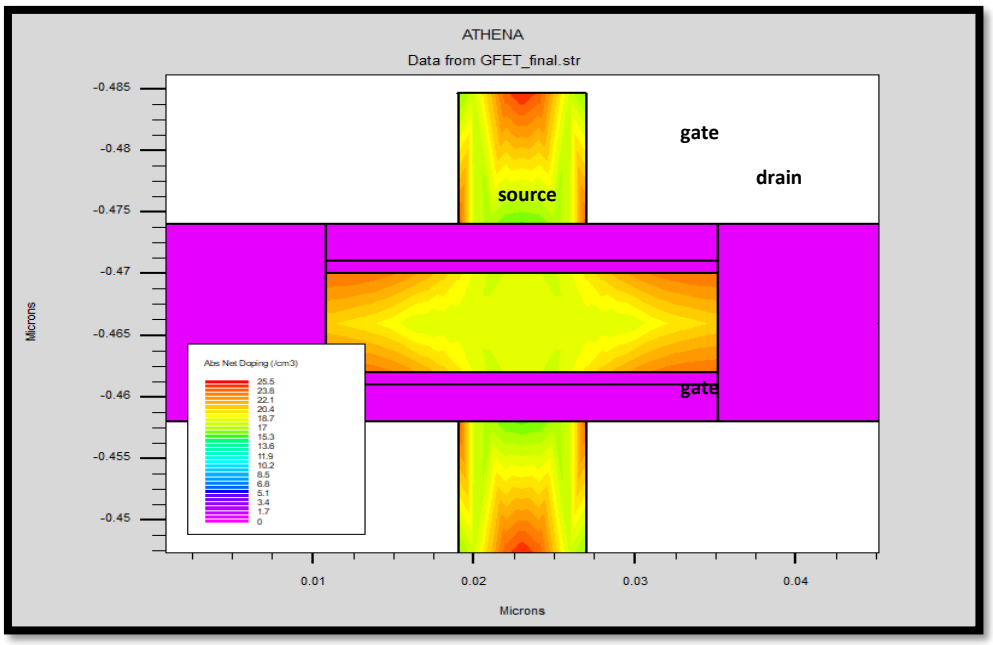


Figure 2. The doping profile of 7.3nm DG-MOSFET virtual transistor

Simulation of Electrical Characteristics

Figure 3 portrays the designed PMOS device's I_{DS}-V_{DS} characteristics while Figure 4 portrays I_{DS}-V_{GS} characteristics. Figure 5 portrays the designed NMOS device's I_{DS}-V_{DS} characteristics while Figure 6 portrays the NMOS devices I_{DS}-V_{GS} characteristics. If the voltage of the gate (V_{GS}) is lesser than the V_{TH}, the drain I_{LEAK} occurs. Comparably, when the transistor, V_{GS}= 0V and V_{DS} = V_{DD} (voltage supply) is turned off, there will be no current in the channel I_{LEAK}.

The baseline simulations give a PMOS threshold-voltage magnitude of 0.2251 V and a reported off-state current of 92.4 nA/µm. While the NMOS threshold-voltage magnitude is 0.2597 V, with a reported off-state current of 93.37 nA/µm.

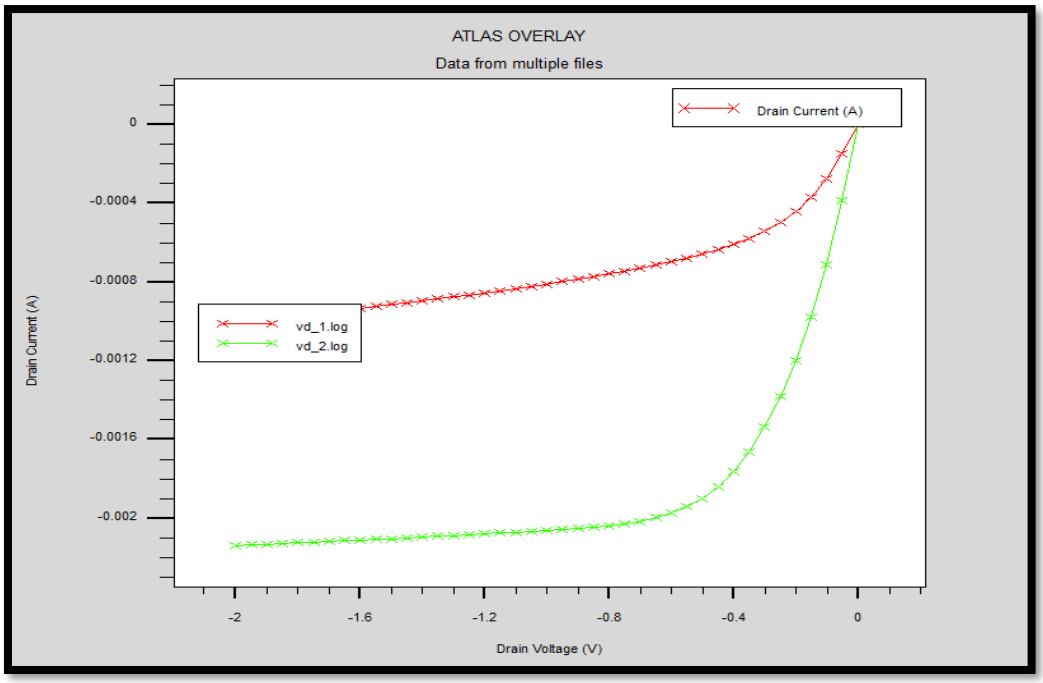


Figure 3. $I_{DS} - V_{DS}$ characteristics of the PMOS device

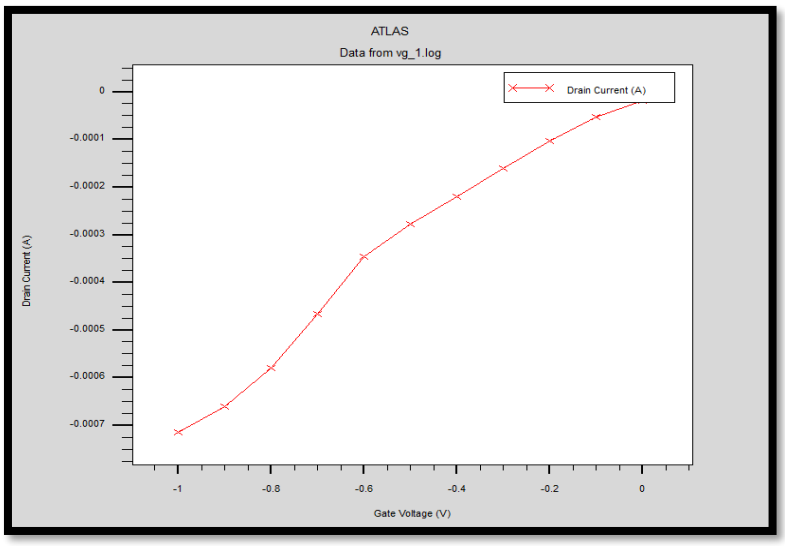


Figure 4. I_{DS} – V_{GS} characteristics of the PMOS device

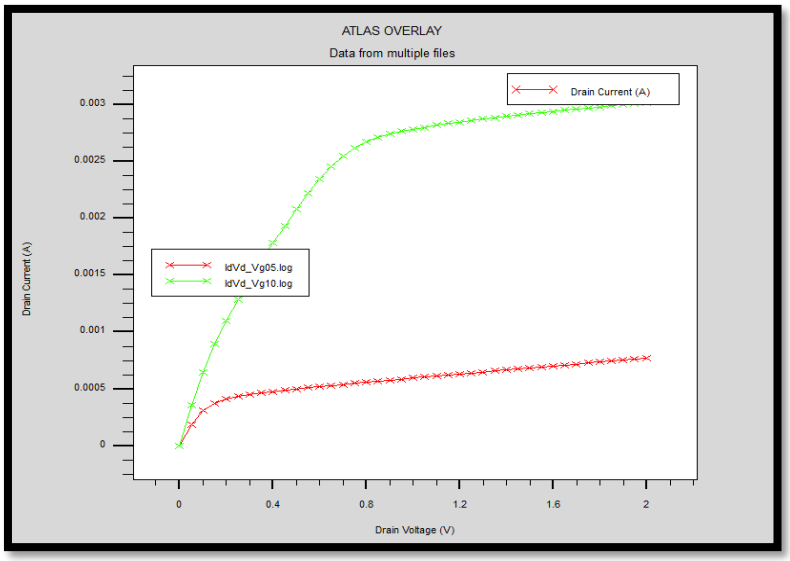


Figure 5. I_{DS} – V_{DS} characteristics of the NMOS device

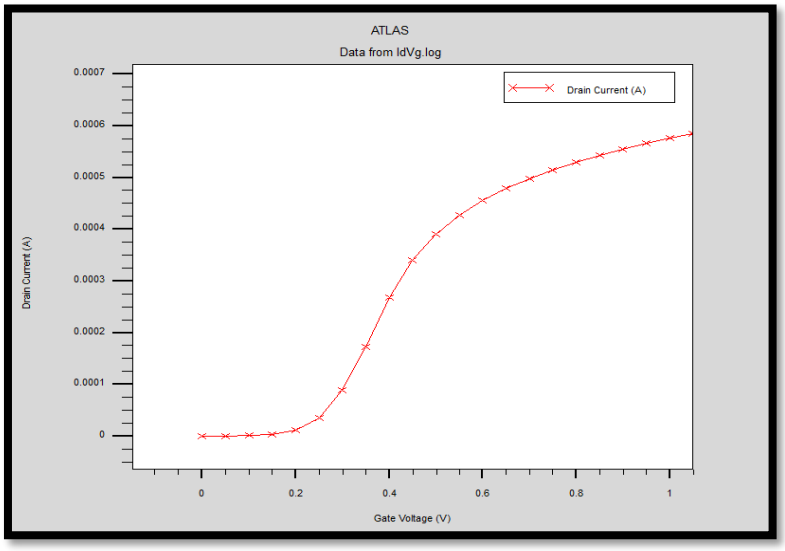


Figure 6. I_{DS} – V_{GS} characteristics of the NMOS device

Future Plan Research

Future work will focus on further optimization of the proposed 7.3 nm gate-length double-gate MOSFET by integrating the Taguchi orthogonal array method with Grey Relational Analysis (GRA) to achieve multi-response optimization of key electrical performance parameters, particularly threshold voltage (V_{TH}) and off-state leakage current (I_{OFF}). This approach will help identify the most significant process and device parameters while determining the optimal combination of factors for improved overall device performance. In addition, alternative high-k gate dielectrics, such as HfO_2 and ZrO_2, and different metal gate materials will be investigated for comparative performance benchmarking. Further studies will also address fabrication-related challenges, including thermal stability, interface quality, and process-induced variability. Moreover, device scalability towards industrial production, including fabrication cost and manufacturing yield, will be explored to assess the practical feasibility of the proposed structure. Other performance metrics, such as carrier mobility, subthreshold swing (SS), and energy efficiency, will also be investigated to provide a more comprehensive evaluation of device performance and optimization.

CONCLUSION

In a nutshell, it can be concluded that the proposed device has been successfully designed, virtually fabricated, and simulated. The present study establishes the virtual-fabrication baseline and evaluates the initial V_{TH} and I_{OFF} characteristics of the proposed device. Future work will focus on the systematic optimization of device and process parameters to further improve V_{TH} and I_{OFF} performance, which will be presented in a subsequent publication. The Taguchi orthogonal array method will be employed to identify the parameters with the greatest influence on V_{TH} and I_{OFF}, thereby facilitating the refinement of the device design and electrical performance.

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