Heat Sink Geometry Comparison for Energy Efficiency in Compact Electronics: Implications for Electricity Savings and CO_2 Emission Reduction

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ABSTRACT

The rising global demand for digital technology has increased electricity consumption across all levels of electronic usage, from household devices to large-scale data centers. Improving the energy efficiency of compact electronics is therefore essential for reducing power demand and lowering the CO_2 emissions associated with electricity generation. This study compares two copper heat sink geometries—fin-type and pin-type—to evaluate their influence on thermal management and energy-use effectiveness in a miniature Application-Specific Integrated Circuit (ASIC) device exposed to laminar airflow for heat dissipation. Laminar airflow at a speed of 0.5 m/s was selected to simulate typical compact electronic ventilation. Using infrared thermography and onboard sensing, the study examines how geometric variations affect heat dissipation, operational temperature, and computational efficiency under a constant 100 W load. Results show that the 9-pin heat sink significantly reduces MOSFET temperature and increases computational output compared to both the 3-fin design and baseline conditions without a heat sink. These improvements translate into lower thermal losses, enabling the device to operate more efficiently with reduced electrical strain. By demonstrating that simple, low-cost geometric enhancements can meaningfully decrease heat accumulation and improve energy efficiency, this research highlights a practical pathway for reducing electricity consumption and the associated CO_2 emissions generated from fossil-fuel-based power systems. Moreover, the design insights are supported by recent advances in pin-fin design and optimization, reinforcing their relevance for sustainable electronics.

INTRODUCTION

The rising global demand for digital technology has increased electricity consumption across all levels of electronic usage, from household devices to large-scale data centers, making energy efficiency in electronics a key lever for reducing power demand and associated CO_2 emissions. Recent assessments show that data-center electricity demand has grown and contributes materially to global electricity use, while uncertainty in estimates underscores the need for device-level efficiency improvements (Mytton & Ashtine, 2022; Khosravi et al., 2024). Improving thermal management in compact electronics reduces electrical losses and auxiliary cooling requirements, directly lowering energy consumption and carbon intensity of operation (Zhang et al., 2022; Noussan et al., 2024). Heat-sink geometry—particularly pin-fin versus plate-fin structures—strongly influences convective surface area, boundary-layer disruption, and heat-transfer efficiency under forced laminar flow, with recent studies reporting consistent performance advantages for optimized pin-fin arrays (Rahman et al., 2024; Yang et al., 2024; Qin et al., 2024; Zohora et al., 2024; Linke et al., 2024; Nawaz et al., 2022). This study therefore evaluates two copper heat-sink geometries (3-fin and 9-pin) under laminar airflow (0.5 m/s) to quantify differences in MOSFET temperature, computational efficiency, and the implied electricity-use and CO_2-reduction benefits when such device-level improvements are scaled.

METHODOLOGY

Two copper heat sink geometries—a 3-fin structure and a 9-pin structure—were fabricated from a 6 mm × 6 mm copper bar using EDM wire cutting. Each heat sink maintained a consistent 36 mm² contact area with the

MOSFET surface to ensure fair comparison. The objective was to evaluate how geometric design influences heat removal efficiency and the resulting impact on device energy performance.

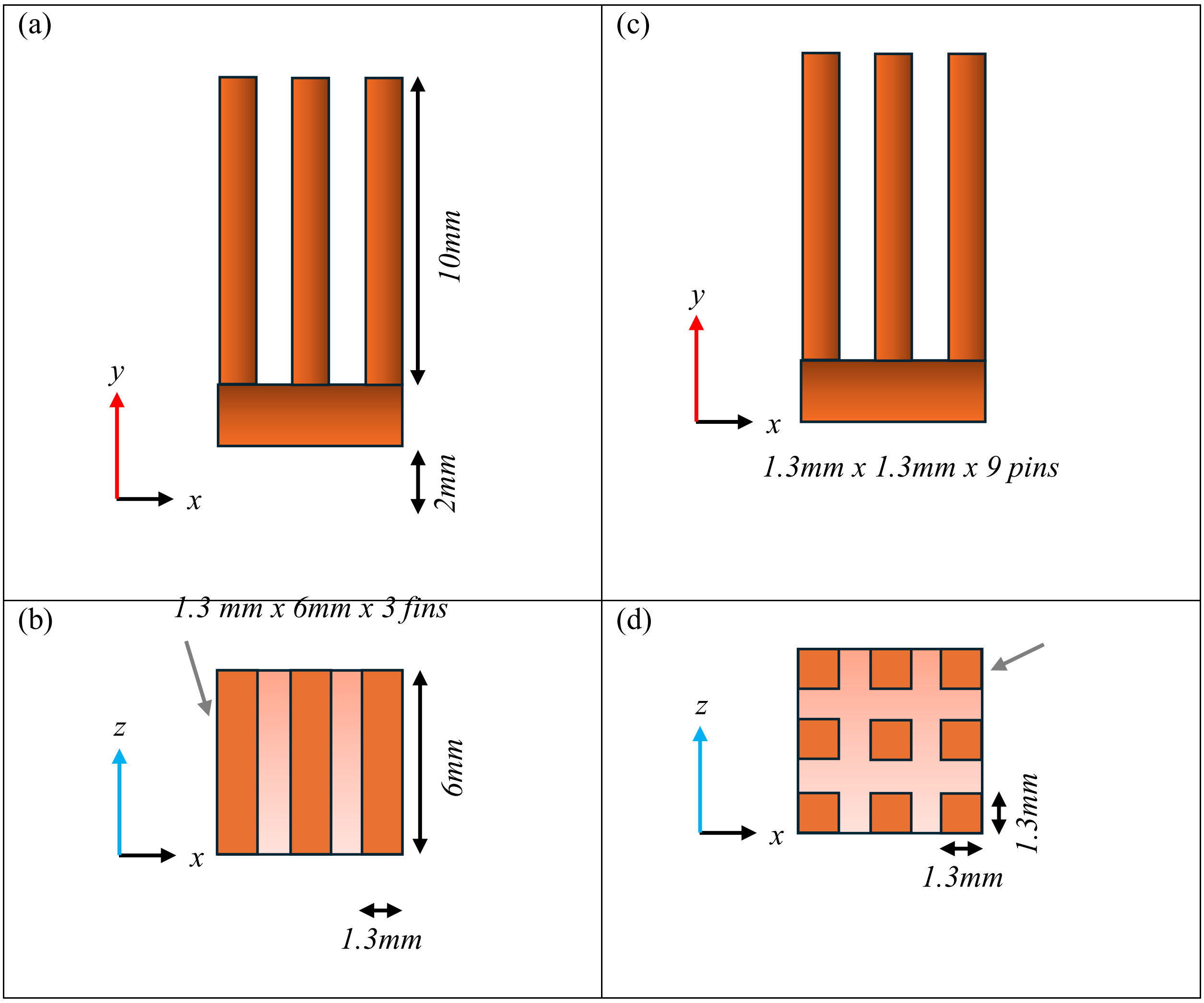

Figure 1: Front view of the 3-fins heat sink (a), top view of the 3-fins heat sink (b), front view of the 9-pins heat sink (c), and top view of the 9-pins heat sink (d)

Experimental Parameters

- **Device:** Computer with application specific integrated circuit (ASIC). It comprises of four distributed MOSFETs (processors) as the heat source.
- **Electrical Load:** Constant 100 W to simulate real operational demand.
- **Airflow:** Laminar flow at 0.5 m/s, representing typical compact electronic ventilation.
- **Measurements:**
  - MOSFET temperature
  - Heat sink temperature
  - Computational efficiency (hashrate, MH/s)

The setup is as illustrated in the Figure 2 below.

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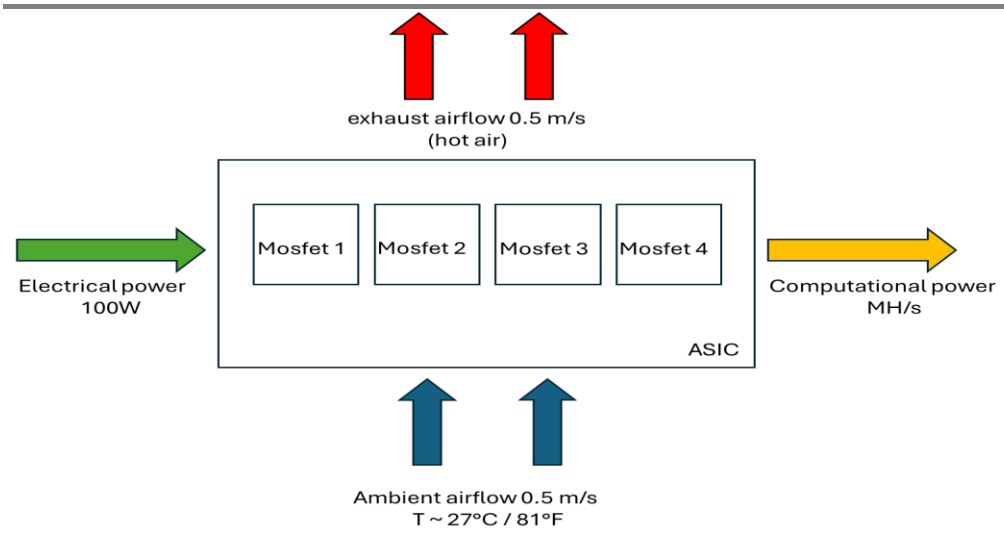

Figure 2: Setup of Application Specific Integrated Circuit (ASIC)

Energy-Related Analysis

- Temperature reductions were used to estimate energy waste reduction, as cooler components require less electrical compensation.
- Hashrate improvements were interpreted as enhanced energy-use efficiency, meaning more useful computation per watt.
- Findings were connected to potential electricity savings and CO_2 emission reductions when applied to large-scale deployments.

RESULTS

Thermal Performance

The 9-pin heat sink lowered MOSFET temperature to 79.1°C, while the 3-fin heat sink reached 87.8°C, and the baseline (no heat sink) peaked at 120°C. These results show that geometric enhancements significantly improved heat extraction. The pin geometry provided more convective surface area, allowing faster heat dissipation under laminar airflow.

Computational Efficiency and Energy Implications

Higher temperatures are associated with electrical losses and performance degradation. The hashrate measurements reflect this:

- **No heat sink:** 202 MH/s
- **3-fin:** 207 MH/s
- **9-pin:** 210 MH/s

This demonstrates that improved heat dissipation enables the device to operate with less internal electrical resistance, meaning more computation per watt of power input. Such improvements contribute directly to electricity savings.

Environmental Impact Evaluation

Efficient heat dissipation reduces electricity consumption in two ways:

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1. Lower electrical losses in overheated components
2. Reduced need for external cooling systems

Assuming large-scale deployment in consumer electronics or computational devices, even small temperature reductions could yield significant reductions in CO_2 emissions. For 9-pin design with 3.81% higher efficiency than the standard, the carbon footprint is significantly lower depending on the fuel used to generate electricity. For a country like Germany that uses lignite, the carbon footprint is the highest at 1.1 kg CO_2/kWh (Table 1). A 3.81% less electricity consumption is generous and lowers the environmental impact significantly.

Table 1: Fuel type and its CO_2 release per kWh electricity generation

Fuel Type	**CO_2 released per kWh (kg CO_2/kWh)**	**Total CO_2 released per GWh (t CO_2/GWh)**
Coal (bituminous/sub-bituminous)	0.820	820
Lignite	1.100	1100
Kerosene (power generation)	0.710	710
Diesel (fuel oil No. 2 / No. 6)	0.740	740
Natural gas (combined cycle)	0.490	490

DISCUSSION

The results show that even simple geometric changes in heat sink design can meaningfully improve thermal performance and energy efficiency. By keeping electronic components cooler, less power is wasted overcoming thermal resistance, and devices can perform more work using the same electricity input.

This has broad implications for sustainability:

- Cooler devices require less auxiliary cooling, reducing electricity consumption.
- Lower energy requirements lead to reduced CO_2 emissions, especially in regions where electricity is lignite, coal or gas-powered.
- Enhanced device efficiency prolongs hardware lifespan, reducing electronic waste.
- At scale - such as in data centers, mining rigs, or edge computing, optimized cooling solutions can contribute to national and global energy-saving strategies.

CONCLUSION

This study compared fin and pin heat sink geometries for improving heat dissipation, energy efficiency, and environmental performance in compact electronic devices. The 9-pin design demonstrated superior thermal conduction and convection under laminar airflow, reducing mosfet temperature and increasing computational efficiency.

By lowering device temperature, electrical losses were minimized, resulting in improved energy-use efficiency. When such improvements are applied across large populations of electronic devices, the cumulative effect translates into meaningful electricity savings and CO_2 emission reductions.

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