Power Optimized Gate Finfet Based SRAM Cell Design to Enhance the Read Access and Improve the Writing Speed

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ABSTRACT

Multi-port SRAM is important for storing, sharing data quickly into the modern processors. This study focuses on 6T SRAM cells designed with 7nm FinFET technology, which is known for its fast operation, low power usage, and high efficiency compared to traditional CMOS designs. The performance of these SRAMs was tested under various conditions, including supply voltages from 0.1V to 1.0V and frequencies ranging from 10 MHz to 2 GHz, using the Microwind 3.8 simulation tool. Key metrics like write time, access time, and power consumption were analyzed, showing that FinFET-based designs perform better overall, making them a great choice for modern electronic systems.

Keywords: SRAM; FinFETs; Multi-port; Write Time; Read Time; Power

INTRODUCTION

High-speed multi-port embedded memories are essential in modern microprocessors and SoCs because they allow multiple read or write operations at a time. However, traditional SRAM using planar CMOS faces problems lead to higher leakage currents and lower threshold voltages [1]. In multi-port SRAMs, these challenges worsen as more ports are added due to increased leakage, parasitic capacitance, and bit line complexity. While some techniques can address these issues, they are not sufficient to fully overcome the limitations of CMOS scaling.

FinFET technology offers significant advantages for SRAM design. First, its Independent Gate mode allows better control of the threshold voltage, improving read and write performance. Second, FinFET's high on/off current ratio, achieved through better short-channel control, helps reduce standby power [2]. Third, its small parasitic capacitance reduces the load on bit lines, which decreases the time required for read and write operations. These features make FinFET a better alternative to traditional CMOS for SRAM designs.

Despite these benefits, improving read or write performance in multiport FinFET SRAMs remains challenging. Multi-port SRAM designs are typically classified into two structures. One of the design uses two bit lines for each port, while another design uses only one [3]. One bit line SRAM which has isolated read ports can address issues like destructive reads (where internal nodes are disrupted) and reduce read times. Additionally, eliminating one bit line in this design reduces area and wiring complexity. However, this designs face difficulties in breaking the loop between the two inverters in the SRAM, which increases the write delay. Balancing these trade-offs is key to optimizing multi-port FinFET SRAM designs.

LITERATURE SURVEY

In 2019, a 11T SRAM cell was introduced using FinFET with double-gate FETs [4]. This design builds on the traditional 6T SRAM but includes four NMOS transistors to stabilize and reduce leakage power. A special header scheme with an extra PMOS transistor is used to enhance read and write stability. This design helps reduced leakage current, shorter write time, and improved read operations. The cell performs well at both high and low voltages, making it a great option for low-power applications.

In 2022, a comparative study of different FinFET-based SRAM designs was published [1]. This study analyzed FinFET SRAM related to power consumption, delay, and stability. The research also included simulations of five

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transistor and six transistor SRAM designs using both CMOS and FinFET at 14nm in the Microwind tool. The results showed that FinFET-based SRAMs perform better than traditional single-channel transistors by solving issues like short-channel effects, leakage, and low voltage operation.

A study from 2013 explored multiport FinFET SRAM [5] designs, including two-bit line for each port and one bit line for each port. Multiport FinFET SRAM showed better performance, reduced leakage current, shorter write time, and also improved read operations. This design also provides more flexibility in configuring read acceleration while maintaining good stability.

In 2014, a study introduced two new 6T SRAM using independently controlled gate FinFET [6]. These new designs separate the read and write lines to improve speed and reduce read-time delay. The study found that these designs reduced leakage current by over 80% and significantly improved read and write performance. These SRAM cells can be easily scaled for larger circuits and allow separate read and write operations.

Another study in 2014 introduced a low-power multi-port SRAM. This structure helps to reduce disturbances during write operations and improves SNM [7]. This design reduces the number of transistors per cell, making it more compact and power-efficient.

In 2017, a study presented a fully functional 4kb, 8-port SRAM designed for low-voltage shared memory systems [8]. This design offers high system throughput and improved read stability by isolating read ports. Simulations showed that at a 0.4V supply voltage, the 8-port SRAM achieved good noise margins for reading, writing, and standby modes. The study confirmed that the design met goals for stability, performance, power efficiency, and area reduction.

Proposed Work

The conventional 6T SRAM cell uses the same bit line for both read and write data, the Fig. 1 shows block diagram of 6T SRAM[9]**.** It consists of a word line and bit lines for data operations. During a write, the pass transistor M5 and M6 are turned on because the word line is kept high. The bit linevalues depend on the value in the cell, while switching transistors M3 and M4 are controlled by the stored values at Q and QB. This design is efficient for basic read/write operations but can face challenges when additional ports are needed for simultaneous both read and write operations.

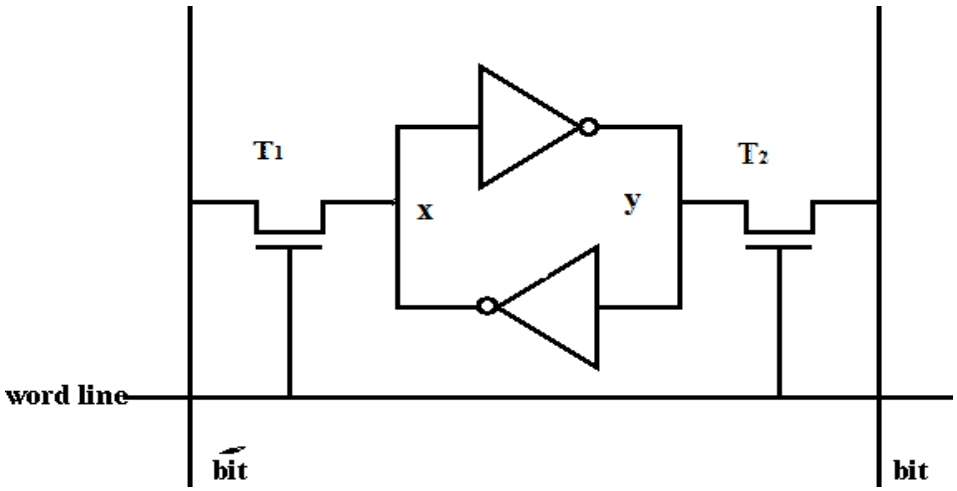

Fig. 1 Block diagram of 6T SRAM

The 6T SRAM using FinFET is shown in Fig. 2, for enhanced performance and flexibility. The 10T SRAM with 2 write ports and 1 read port is shown in Fig.3. It builds on the structure of 6T SRAM cell, retaining the transistor M5 and M6,[5] which remain on during write. The additional read transistors, M7 and M8, are used specifically for read operations. These transistors are configured to Vss during read operations and to supply voltage during write and hold modes. This configuration helps control the bit line leakage current, improving power efficiency.

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During a write, the write-word line is on, while the read-word line is off. Assume the initial data at node Q is logic 0, and we need to write logic 1 at this node. In this case, the bit line is high, and the complementary bit line is very low. The old logic 1 stored at the opposite node is get to the access transistor M6 and switching transistor M 4. Meanwhile, the new logic 1 is charged to V_{dd} through transistors M5 and M1, [10]as the switching transistor M3 is turned off to prevent further discharging. To improve the write margin during this, the PMOS transistor is set to a power supply. Additionally, the virtual ground is kept Vdd**,** which reduces potential leakage paths .

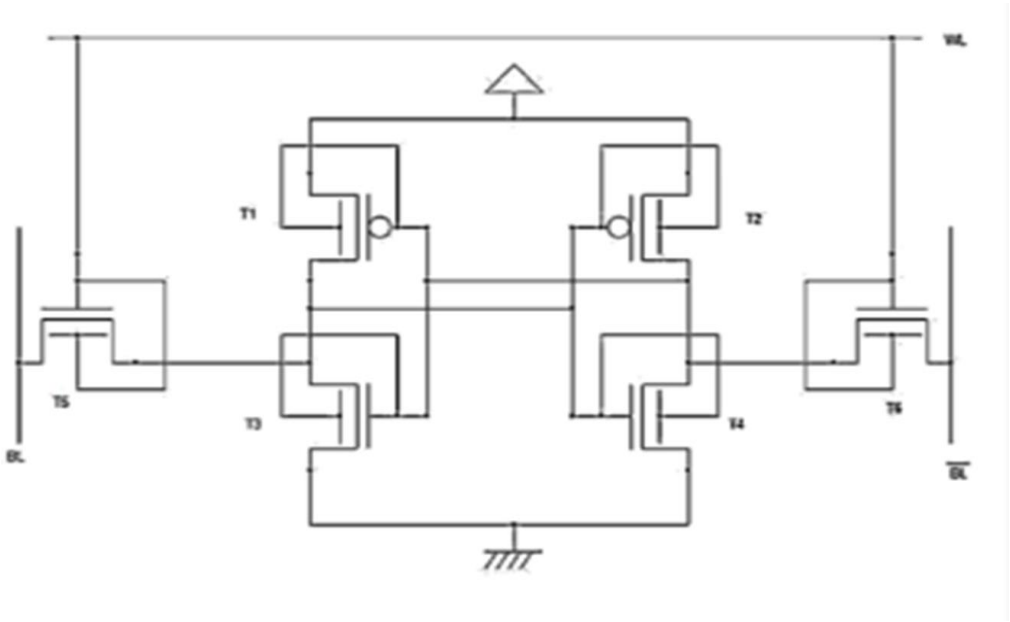

Fig.2: 6T SRAM using FinFET

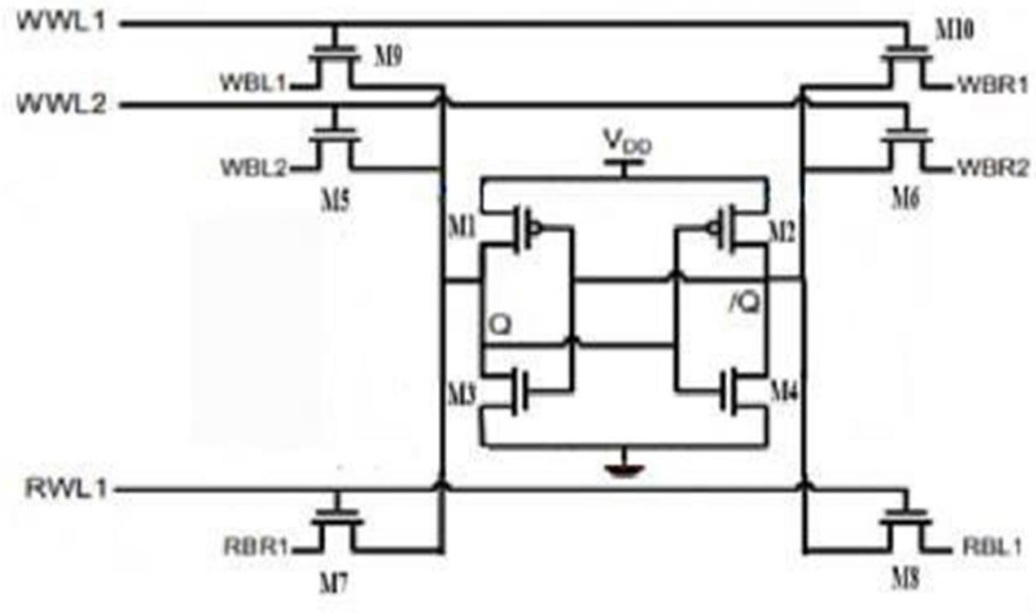

Fig.3: 10T multiport SRAM

During a read, the read-word line kept on, and the write- word line is off. Bit lines are connected to the supply before the read starts. Since the stored value at node Q is low and word line is also low, the pass transistors M5 and M6[11] turned off. however, allowing the stored data at node Q to be transmitted to the read bit lines. This design ensures that the read operation does not disturb the stored data in the SRAM cell.

In hold operation, both the read-word lines and write-word lines are turned off. This configuration prevents any potential leakage paths between the bit lines, thereby reducing leakage power. The hold operation ensures that the stored data remains stable without any unnecessary power loss.

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The layout of 6T SRAM using FinFET is shown in Fig.4. The proposed 10T SRAM design improves the efficiency compared to the conventional 6T design. The layout of 10T SRAM cell using FinFET is shown in Fig.5.[12] By separating the read and write ports, it minimizes conflicts during simultaneous operations. The use of a virtual ground at Vdd and controlled transistor operations reduces leakage power and enhances overall performance. This design is especially suitable for modern multi-core processors and SoCs, where power efficiency and reliability are critical.

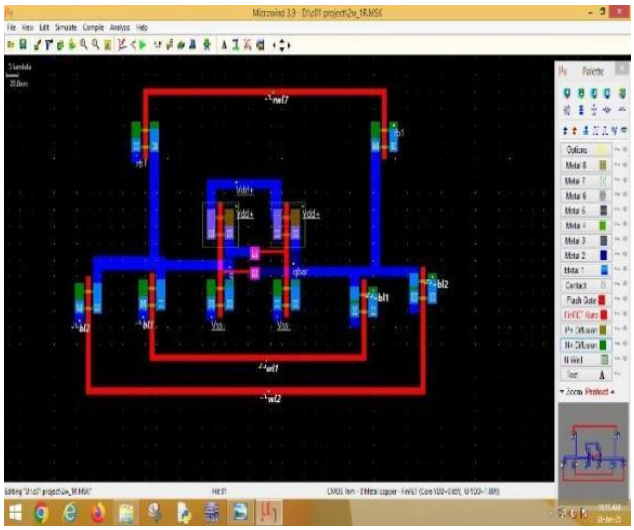

Fig.4 : Layouts of 6T SRAM

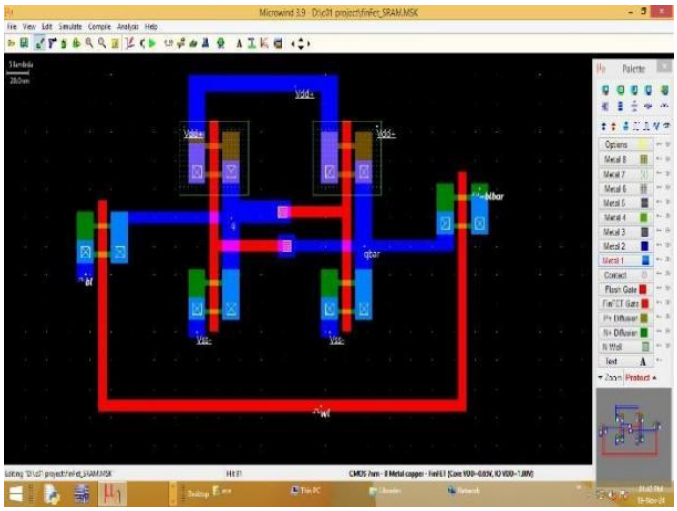

Fig.5: Layout of 10T SRAM

A 6T SRAM cell is a fundamental building block of static random-access memory, consisting of six transistors arranged in a rectangular layout. At the heart of the 6T SRAM cell are two cross-coupled inverters, which form the storage nodes that hold the binary data. These inverters are designed to provide a stable and robust storage mechanism, allowing the SRAM cell to maintain its state even when power is applied. In addition to the cross-coupled inverters, the 6T SRAM cell also includes two access transistors, which control the flow of data into and out of the cell during read and write operations.

10T SRAM cell includes four additional transistors, which are used to implement a read buffer and a write driver. These additional transistors result in an L-shaped layout, which provides improved read stability and writability compared to the 6T SRAM cell. The read buffer is designed to isolate the storage nodes from the read path, reducing the impact of read disturbances and improving the overall stability of the SRAM cell. Similarly, the write driver provides a stronger write signal, making it easier to write data to the SRAM cell and improving the overall writeability. These improvements make the 10T SRAM[3] cell more suitable for low-voltage and high-density applications, where read stability and writeability are critical.

The additional transistors in the 10T SRAM cell provide several benefits, including improved read stability, writeability, and low-voltage operation. The read buffer and write driver work together to ensure that the SRAM cell can operate reliably even at low supply voltages, making it an attractive option for power-constrained applications. Furthermore, the 10T SRAM cell is also more suitable for high-density applications, where the ability to reliably read and write data is critical. Overall, the 10T SRAM cell offers a number of advantages over the 6T SRAM cell, making it a popular choice for a wide range of applications.

RESULTS

The proposed 10-transistor SRAM cell was simulated using the Microwind tool with FinFET technology at 7nm, operating at room temperature and standard process conditions. The simulation was conducted across a range of voltages, from 0.1V to 1V, to analyze its performance under different conditions. This allowed the evaluation of key performance metrics for both low power and high- performance applications. If the cell performs well in the super-threshold range, it is suitable for high-performance systems, while good performance in the sub-threshold range makes it ideal for low-power applications.

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The proposed cell is observed in a 7nm technology and at a room temperature of 27°C. Initially power versus voltage graph is plotted at different constant frequencies. The power points obtained at the voltages ranges from 0.1V to 1.0V and at the constant frequencies ranges from 10MHz to 2GHz.

Fig.6: Output waveforms of SRAM cells

The images show simulation waveforms from a circuit design tool, likely Microwind. These waveforms help engineers analyze how a circuit behaves over time. The top white waveform is a clock signal**,** which controls the circuit's timing by switching between high and low states. The green and yellow waveforms represent data or control signals**,** which change based on the clock. The red waveform at the bottom shows current consumption, increasing in steps as the circuit operates. This indicates power usage changes due to switching activity**.** The left image includes simulation settings and measurements, while the right image is a closer view of the waveforms. These waveforms help engineers check timing, power, and signal integrity before manufacturing a chip, ensuring efficient and error-free circuit design. In a 6T SRAM cell, this transition can be slow and may exhibit some glitches or ringing due to the RC delay and coupling capacitance. In contrast, the output waveform of a 10T SRAM cell shows a faster and more stable.

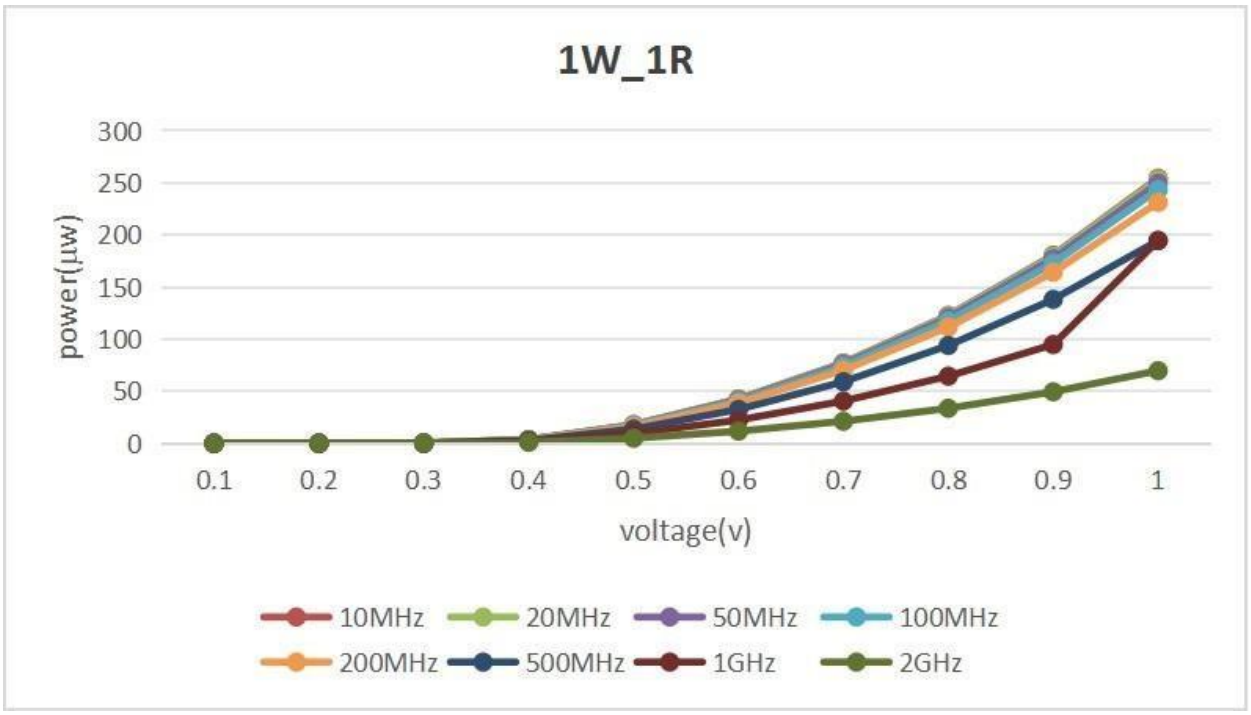

Fig.7 : Power vs Voltage plot of 1W1R SRAM

Power vs Voltage plot of 1W1R SRAM is shown in Fig.7 we can see that the power vs voltage plot of a

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conventional 6T SRAM with 1 write and 1 read port. The power increases with increase in the voltage. At lower frequencies, the curve is increasing exponentially and exhibits nearly same characterstics. At higher frequencies the power consumption is less compared with the lower frequencies. The power increases non-linearly with voltage for all frequencies. This trend reflects the quadratic dependence of dynamic power on voltage, as power $\propto V^2$.The graph shows how power changes in a circuit as voltage and frequency increase. The voltage ranges from 0.1V to 1V, and power is measured in microwatts Different lines in the graph represent different frequencies, from 10 MHz to 2 GHz.

At low voltages (0.1V - 0.5V), the power used is very small and almost the same for all frequencies. When the voltage goes above 0.5V, power usage increases quickly, especially at higher frequencies. Usually, higher frequencies use more power because the circuit switches faster. This pattern is clear in the graph, where 200 MHz, 500 MHz, and 1 GHz show a big jump in power usage at higher voltages. However, something unusual happens at 2 GHz. It uses less power than expected compared to mid-range frequencies. This could be due to better design, lower activity, or other efficiency improvements. The main point from this graph is that power does not increase in a straight line with voltage. A small increase in voltage can lead to a big jump in power usage. This is important for circuit designers, who must balance speed and power efficiency in high-speed.

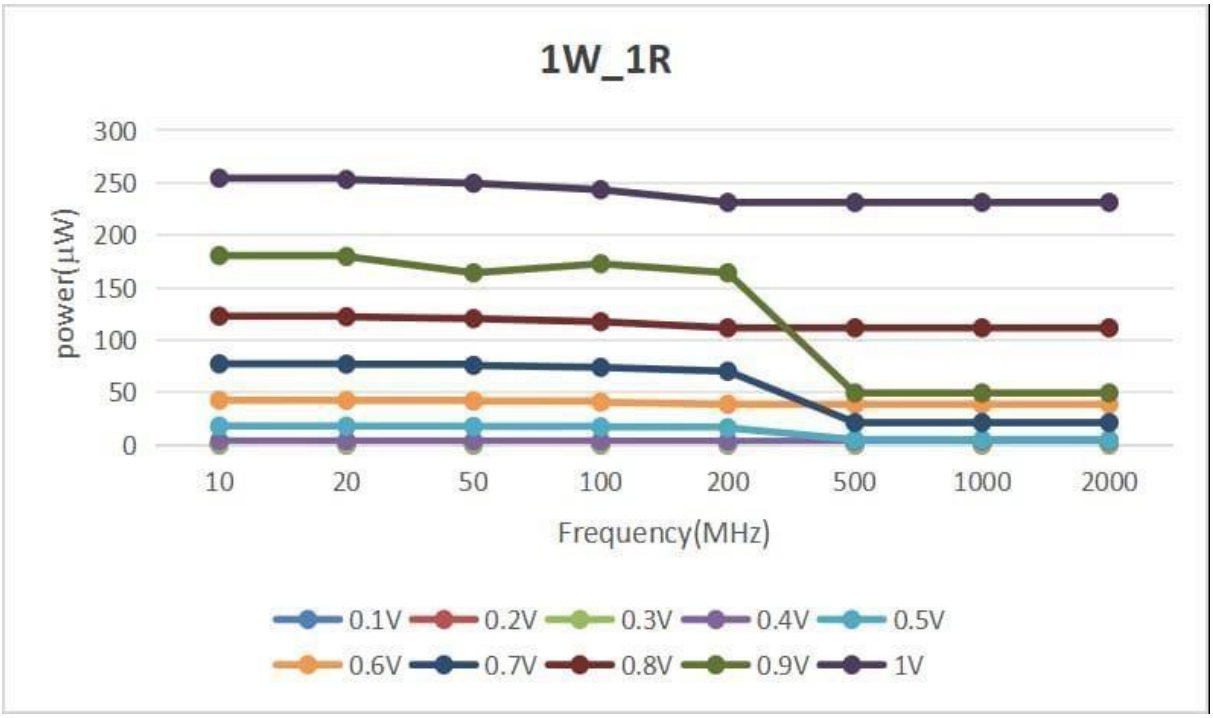

Fig.8 : Power vs Frequency plot of 1W1R SRAM

Power vs Frequency plot of 1W1R SRAM is shown in Fig.8, we can see that the power vs Frequency plot of a conventional 6T SRAM with 1 write and 1 read port. The power decreases slightly with increase in the frequency. At lower frequencies, the curve is constant and exhibits nearly same characterstics. At higher frequencies the power consumption is slightly decreased when compared with the lower frequencies. Lower voltages minimize power dissipation, showcasing the energy- efficient operation of the SRAM. The graph shows how power changes when the circuit runs at different frequencies and voltages. The x-axis represents frequency, from 10 MHz to 2 GHz. The y-axis shows power in microwatts. Each colored line represents a different voltage, from 0.1V to 1V. At low frequencies (10 MHz - 100 MHz), power stays almost the same for each voltage. Higher voltages use more power than lower ones.

At 500 MHz, something different happens. Power suddenly drops, especially for higher voltages like 0.8V, 0.9V, and 1V. After this drop, power remains steady up to 2 GHz. This means the circuit uses less power at higher frequencies, which is unusual. Normally, higher frequencies need more power because the circuit works faster. But in this case, power drops and then stays constant This is important for designing efficient circuits. Engineers

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can use this information to make faster and low-power electronic devices. This is useful for processors, memory chips, and communication systems. The graph shows that higher frequencies do not always mean more power usage. Understanding this helps in balancing speed and power efficiency

The power consumption of 1W-1R SRAM increases with frequency, with several key factors contributing to its power usage. Higher frequencies result in increased power consumption, while lower supply voltages have the opposite effect, reducing power consumption. Additionally, both bitline and wordline capacitance play a significant role, with higher capacitance values leading to increased power consumption.

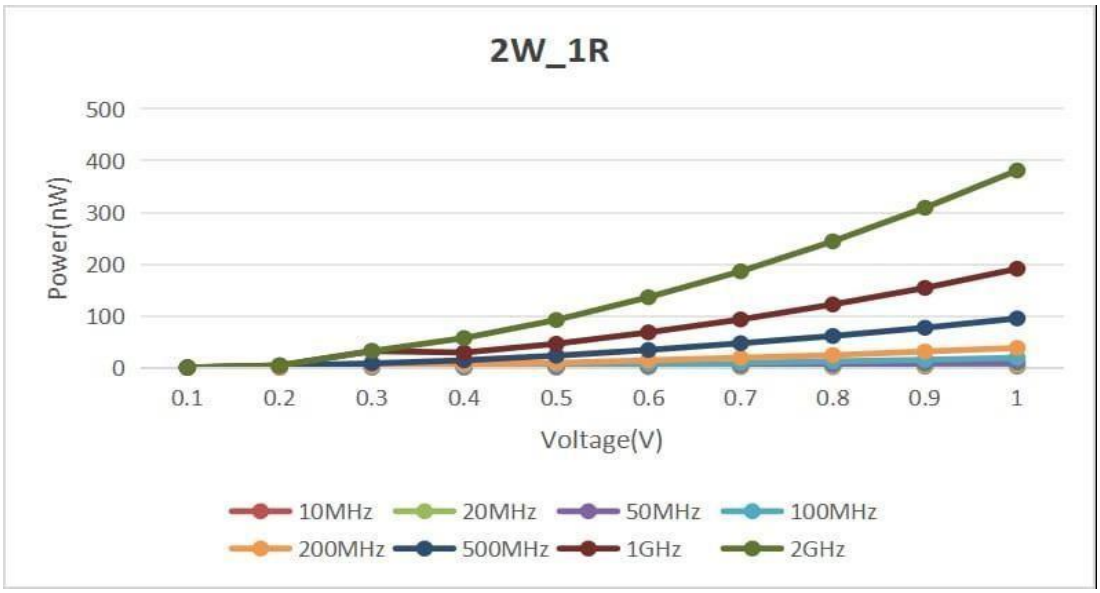

Fig.9 : Power vs Voltage plot of 2W1R SRAM

Power vs Voltage plot of 2W1R SRAM is shown in Fig.9, we can see that the power vs voltage plot of a proposed 10T SRAM with 2 write and 1 read port. The power increases non- linearly with voltage for all frequency levels. At lower voltages, the power consumption is minimal and gradually increases. Beyond 0.6 V, the power rises significantly, especially for higher frequencies. Higher frequencies exhibit substantially higher power consumption compared to lower frequencies. The observed behaviour aligns with the dynamic power formula, $P \propto f \cdot V^2$, where power depends on both frequency and the square of the supply voltage. Lower voltage levels can significantly reduce power consumption, even at moderate frequencies.

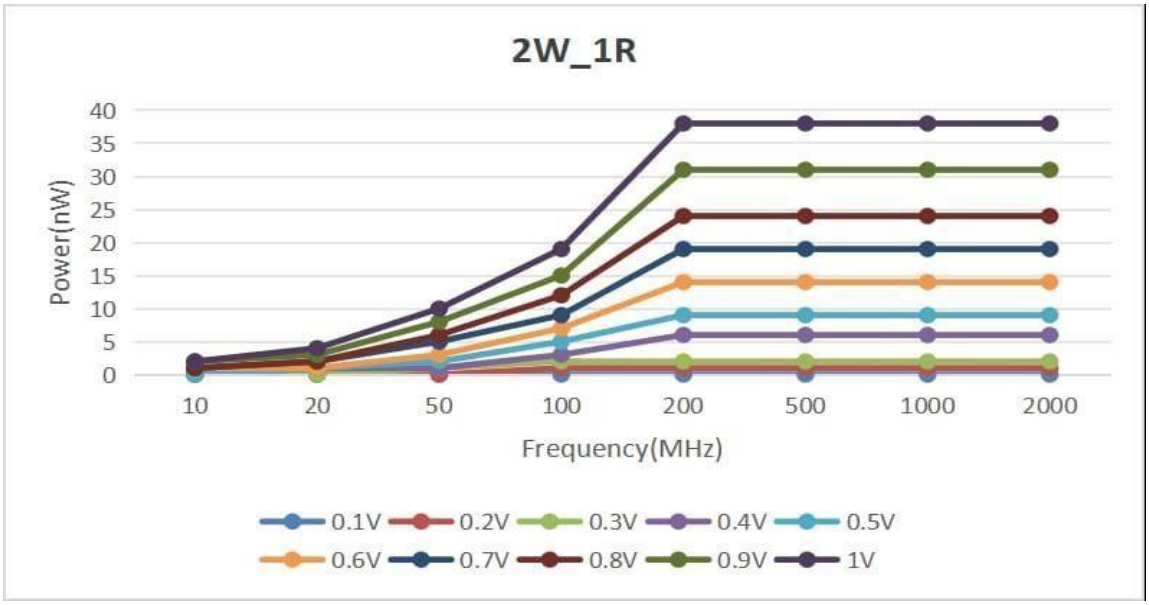

Fig.10 : Power vs Voltage plot of 2W1R SRAM

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Power vs Voltage plot of 2W1R SRAM is shown in Fig.10 we can see that the power vs voltage plot of a proposed 10T SRAM with 2 write and 1 read port. This graph Demonstrates the behaviour of multi-write SRAM cells under high- frequency workloads. Power consumption increases with frequency for all voltage levels. At higher voltages, power consumption is significantly higher than at lower voltages. Beyond 500 MHz, the power stabilizes or saturates for most voltage levels. Saturation could indicate a limit in dynamic power contribution or a shift in the dominant power consumption mechanism (e.g., leakage power). The parameters like read time, write time and power consumption of the conventional SRAM cell is compared with the 6T SRAM using FinFET and proposed 10T SRAM cell and plotted as shown in Fig.11.

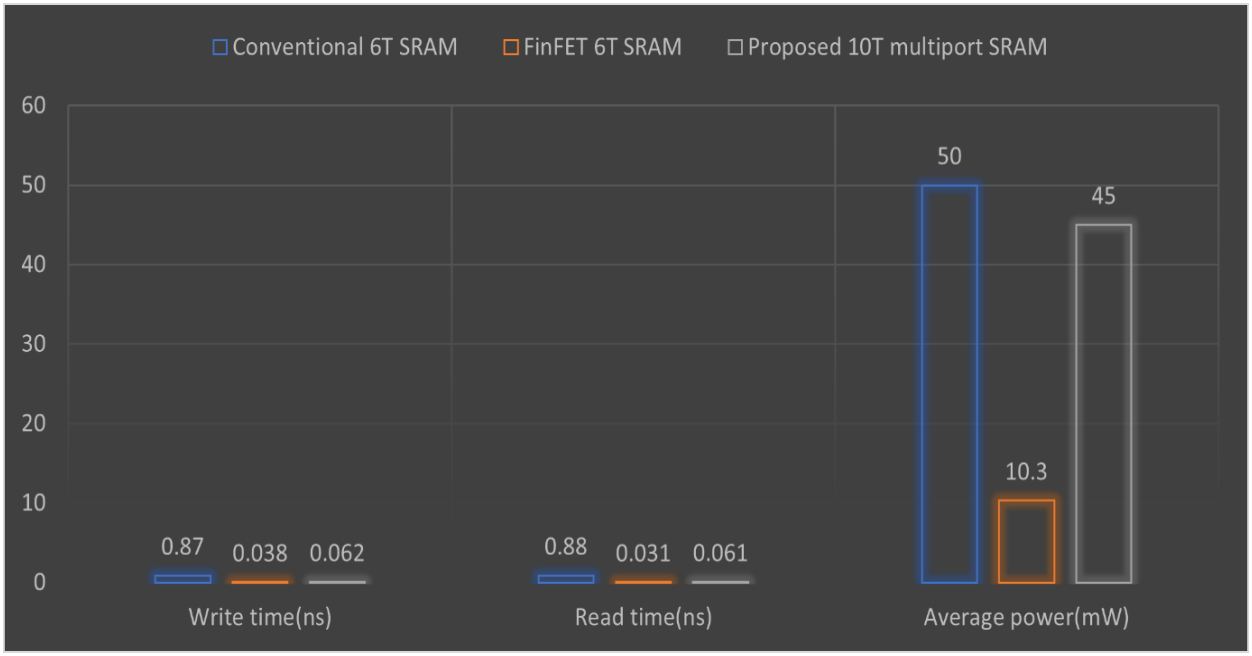

Fig.11: comparison of different parameters of SRAMs

The performance of Power-Optimized Gate FinFET-based SRAM is affected by process variations, temperature changes, and stability issues. Process variations cause shifts in threshold voltage, changes in fin size, and variations in leakage current, leading to unstable read and write operations and higher power consumption. Temperature fluctuations further impact performance by reducing electron mobility, increasing leakage current, and shifting threshold voltage, making the circuit slower and less efficient. Stability issues arise due to changes in read/write margins and data retention problems, increasing the risk of errors and failures. To overcome these challenges, designers use adaptive biasing, assist circuits, and variation-aware simulations to enhance speed, power efficiency, and overall reliability in SRAM designs.

A comparative study of Power-Optimized Gate FinFET-based SRAM shows significant advantages over traditional 6T CMOS SRAM and other advanced SRAM architectures like 8T and 10T designs. While conventional 6T SRAM suffers from high leakage power and stability issues, FinFET-based SRAM reduces leakage and improves read and write speeds. The 8T SRAM offers better read stability but increases area usage, whereas the proposed 10T SRAM further enhances read access, write speed, and power efficiency, making it ideal for low-power, high-performance applications. Looking ahead, future research can focus on ultra-low power designs, variation-tolerant architectures, and 3D-integrated SRAM to improve efficiency and reliability. Additionally, AI-driven optimization can help fine-tune circuit parameters for better performance. These advancements will make FinFET-based SRAM more suitable for next-generation computing systems, including mobile devices, IoT applications, and high-speed processors. SRAMs with 1T-1C (1 Transistor-1 Capacitor) configuration exhibit higher cell density and lower leakage power compared to 6T (6 Transistor) SRAMs, but suffer from lower noise margins and stability. In contrast, 6T SRAMs offer better noise immunity and stability, but at the cost of lower cell density and higher leakage power. Meanwhile, 8T (8 Transistor) SRAMs strike a balance between cell density, noise margin, and leakage power, making them suitable for high-performance applications. Additionally, 1W-1R (1 Wordline-1 Read) SRAMs have lower power consumption and faster access times compared to 1T-1C SRAMs, but require more complex peripheral circuits.

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CONCLUSION

The performance of FinFET 6T SRAM and the Proposed 10T Multiport SRAM compared to Conventional 6T SRAM in respect of write time**,** read time, and power consumption. The FinFET 6T SRAM demonstrates a significant power reduction of 79.4% while achieving an impressive reduction of 85.63% in write time and 86.48% in read time**,** making it the most efficient choice in terms of both speed and energy efficiency. The Proposed 10T Multiport SRAM achieves a 10% reduction in power consumption, with 82.87% faster write time and 83.07% faster read time compared to conventional 6T SRAM. Despite a slightly higher power consumption than FinFET SRAM, it offers multiport access, making it suitable for high-performance applications requiring parallel data operations. These results indicate that FinFET-based SRAM architectures significantly enhance speed and power efficiency, while the 10T multiport SRAM offers a balanced trade-off between speed and multiport functionality. These findings contribute to the development of low-power, high- speed memory architectures for next-generation computing systems.

Designing a Power-Optimized Gate FinFET-based SRAM cell has some challenges. The area of FinFET SRAM is larger than traditional CMOS because of its multi-gate structure. To save space, designers must optimize the layout. Fabrication is also complex due to lithography, fin patterning, and alignment issues. Advanced manufacturing techniques help in reducing errors. Process variations like threshold voltage shifts and temperature effects can affect read and write stability. To solve this, designers use assist circuits, adaptive biasing, and simulations. These methods improve speed, reduce power consumption, and increase reliability. With these solutions, FinFET SRAM can work well for modern memory applications.

The conventional 6T SRAM cell**,** FinFET-based 6T SRAM, and proposed 10T multiport SRAM differ in power, stability, speed, and area. The 6T SRAM is compact but suffers from high leakage power, read stability issues, and limited write ability due to shared read/write paths. The FinFET-based 6T SRAM improves power efficiency, speed, and stability due to better gate control and reduced leakage. However, both designs are single-port, allowing only one read/write operation at a time. In contrast, the proposed 10T multiport SRAM introduces separate read/write ports**,** enhancing read stability and write ability while reducing interference. It also supports multiple simultaneous accesses, making it ideal for high-speed computing. Though it requires more area, its lower power consumption and improved performance make it suitable for advanced memory applications.

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