Memory Circuits Used in Digital VLSI: Comparison

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Abstract: **Note on differences between different semiconductor volatile and non-volatile memory. Comparison is done for parameters such as volatility, read & write speed, structure and power dissipation. Based on the parameters compared applications for these memory cells has been detailed. The paper helps to make a choice based on the application and comparison made.**

I. INTRODUCTION

Semiconductor memory cells are adept for storing huge digital data, required for digitized systems. It is a vital component in current technical world. Due to rapid growth and requirement for faster memories, various types of semiconductor memories have been emerged. The two different types of memories are Volatile memory (holds the data only when the device is on) and non-volatile memory (holds data even when the device is off).

1. Volatile memory

Volatile memory requires power supply to sustain the information; it preserves its data while powered but loses the data when power supply is interrupted. Even though volatile memory loses its data while power is interrupted, being a faster memory has various uses such as primary memory in computers, volatile memory can safeguard delicate information, since the data cannot be obtained once the device is turned off.

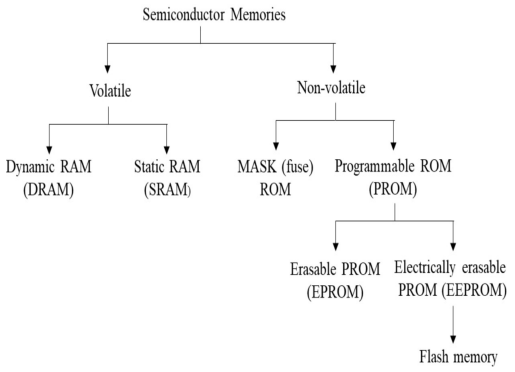

Figure 1

Dynamic Random Access Memory

Dynamic random-access memory stores one bit of data in different capacitor in the integrated circuit. The capacitor is charged or discharged depending on the data it holds, the charged and discharged state can be used to represent the two distinct states of a bit each, either 0 and 1

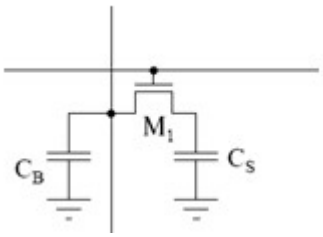

Figure 2

1-bit DRAM circuit shown in Fig 2. The capacitor C_S stores the data for the cell and Read/Write access is given to the cell via Transistor M1. The capacitance for each bit line per length is given by C_B. Cells are etched on silicon wafer as an array with columns representing bits and rows representing a word.

The address of a cell is provided by the junction of a bit and a word. In dynamic random access memory to activate each bit in the column via the transistor a charge is sent. To write, the row lines contain the state that the capacitor should attain. When reading, the charge on the capacitor is sensed via a sense amplifier which gives the level of charge in the capacitor above 50%, the data is a logic "1" or else a logic "0".

It is unacceptable for memory to lose data. The problems with this particular arrangement is that capacitor does not hold its charge indefinitely as there is minor charge leakage. To get around this problem the data is periodically refreshed. The data is sensed and re-written this ensures that any leakage is overcome and the data is not lost. Since the system needs to be continually refreshed to preserve its memory, in spite of being more widely used memory a more complex circuit and timing requirement has been associated with DRAM. Since only one transistor and one capacitor is required to store one bit of memory, this makes the structure of the memory cell simple and allow for very high density which makes the DRAM less expensive per bit compared to other memory cells. The transistors and capacitors used are extremely small; billions can fit on a single memory chip. Since DRAM is a dynamic memory cell it dissipates large amounts of power.

Static Random Access Memory

Static random-access memory is a semiconductor memory which uses bi-stable latches or flip-flops to store one bit of data. Even though SRAM shows data remanence, the data is eventually lost when the cell loses power.

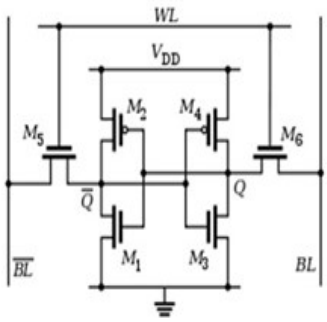

Figure 3 -6T SRAM Cell

Fig 3 shows a typical 6T-SRAM cell. SRAM takes 6 transistors to store a 1 bit. It has three input lines and two output lines. In Figure 5. Transistors M5 and M6 are called access transistors, while transistors M2 and M4 used as pull up transistors and transistors M1 and M3 are used as pull down transistors. SRAM has three operations, namely hold, read and write operation.

Hold operation: During hold Operation both access transistors are turned OFF. SRAM holds its current state due to latching.

Read Operation: During read operation the two bit lines must be recharged to VDD and the access transistors must be turned on. Based on the value stored any one of bit line is discharge and the potential difference between the two bit lines determined by the sense amplifier give the value of the data stored either logic one or logic zero.

Write Operation: The data to be written onto the memory is given to the bit line while the access transistors are in on state Because of its high speed SRAM cells are used as cache memories and as main memory in servers.

2. Non volatile memory

The advantage of Non-Volatile memory over Volatile memory such as SRAM and DRAM is that they do not lose their data in the absence of power. Various Non-Volatile memory have been developed to get around the problem of volatile memory. Non-volatile memory is a computer memory that holds the saved data even when the power is off. Another advantage of Non-Volatile memory over Volatile memory is that, it does not have to be refreshed periodically. It generally used as secondary storage for consistent long term storage. It finds abundant usage in memory chips for USB Drives and Cameras. With higher speeds than the magnetic discs, it is quickly replacing the current Hard Disk Drives as secondary memory in computers

Read Only Memory

Firmware or Read-only memory (ROM), is an IC programmed with data during manufacture. ROM finds its use in many electronic devices.

In Read Only Memory (ROM) the data cannot be deleted or over written by the user. All the data that are supposed to be stored are done so during the manufacturing process. During fabrication of the integrated circuit to store a specific data a ROM Mask which contains the necessary data is used.

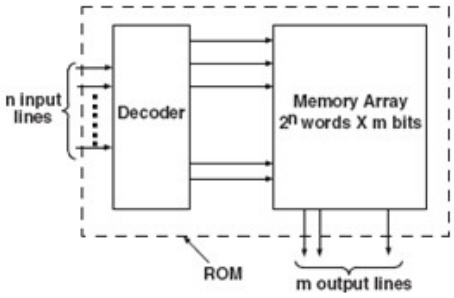

Figure 4- ROM array

Even though having a disadvantage of not allowing its user to modify the data. It servers to protect the data from attackers in vulnerable memory chips.

Rom arrays can be implemented in two different ways

NOR based ROM

NAND based ROM

Programmable Read Only Memory

A read only memory that can be programmed only once by the user. Once purchased the user can store the desired data in the blank PROM chip using a PROM program. To program the data onto a PROM chip, there exists tiny fuses that can be burnt during programming. Once programmed the data cannot be modified or erased since the fuses are already burnt to store the data.

Erasable Programmable Read Only Memory

The data in the EPROM is erased by shining UV light onto the cells via a transparent window in the chip. The UV light makes the oxide conductive generating an electron-hole pair in the material. Depending on the Source of the UV light the erasing process can take from few seconds to several minutes, making the erasing process slow. It takes 5-10 micro seconds per word to program the data. Disadvantage of erasing the data via a UV light is that, the number of times the memory can be erased and reprogrammed is limited, mainly due to UV erase procedure. The threshold on the device may vary with repeated erasing and reprogramming, hence the EPROM is fabricated with an on-chip circuit to control the threshold during programming. The power dissipation during programming is high due to large channel currents and gate voltage being high as 12.5V. voltage of 12.5V. Due to simplicity and higher density of the EPROM cell large memories can be manufactured at a relatively low cost. EPROMs finds its application in devices that do not require regular programming. Due to reliability, Flash memories now replace EPROM's.

Electrically Erasable Programmable Read Only Memory

By exposing the contents of the EEPROM to an electric charge the data in the EEPROM can be erased. The data in the EEPROM is stored or removed by 1 byte at a time. One of the advantages of EEPROM is that additions device is not required to modify the content of the memory. The modern EEPROM can perform multi-byte page operations.

Flash Memory

The flash memory is the most widely used memory in computers and electronic devices. A block of data can be programmed using the flash memory. The flash memory maintains its data even without power. Due to the speed and efficiency of the flash memory it has become even more popular than the EEPROM's with current modules being designed for about 100000 -10000000 write cycles. The main drawback of the flash memory is the number of times data can be written. Even though there are no restrictions on how many times the data can be read from the flash memory, the memory itself fails after a certain number of write cycles

NOR BASED

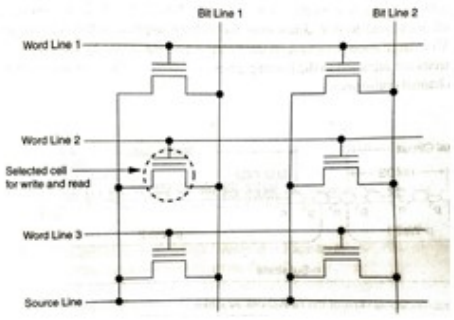

Figure 5 NOR cell configuration

Table 1 – Bias conditions of the NOR cells for erase, programming and read operation

Signal	Operation		
	Erase	**Programming**	**Read**
Bit line 1	Open	6V	1V
Bit line 1	Open	0V	0V
Source line	12V	0V	0V
Word line 1	0V	0V	0V
Word line 2	0V	12V	5V
Word line 3	0V	0V	0V

Fig 6 and table 1 show the NOR cell configuration and bias conditions for erase, programming and read operations, respectively. The NOR cell uses the F-N tunneling mechanism for the erase operation and the hot-electron injection mechanism for the programming operation

NAND BASED

Table 2 – Bias conditions of the NAND cells for erase, programming and read operation

	Operation		
Signal	**Erase**	**Programming**	**Read**
Bit line 1	Open	0V	1V
Bit line 1	Open	0V	1V
Select line 1	0V	5V	5V
Word line 1	0V	10V	5V
Word line 2	0V	10V	5V
Word line 3	0V	10V	5V
Word line 4	0V	10V	5V
Word line 5	0V	20V	0V
Word line 6	0V	10V	5V
Word line 7	0V	10V	5V
Word line 8	0V	10V	5V
Source line 2	Open	0V	5V
Source line	20V	0V	0V
p-well 2	20V	0V	0V
n-sub	20V	0V	0V

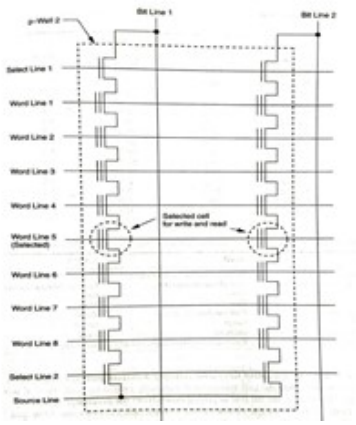

Fig. 6 - Equivalent circuit of the 8 bit NAND cell

Equivalent circuit of the 8 bit NAND cell structure is shown in fig 6. Bias conditions for erase, programming and read operations are shown in table 2. The NAND cell uses an F-N tunneling mechanism for the erase operation.

II. RESULT & CONCLUSION

Table 3-comparison

Parameter	Memory Type	
	DRAM	**SRAM**
Cell Structure	1T-1C	6T
Cell Density	High	Low

Power consumption	High	High/Low
Read Speed	~50 ns	~10/70 ns
Write Speed	~40 ns	~5/50 ns
Cost	Low	High
Application	Main Memory	Cache/PADs

Parameter	**Memory type**		
	EPROM	**EEPROM**	**FLASH**
Cell structure	1 T	2 T	1 T
Cell Density	High	Low	High
Power consumption	Low	Low	Low
Read speed	~50 ns	~50 ns	~50 ns
Write speed	~10 µs	~5 ms	~(10 ns-1ms)
Cost	Low	High	Low
Application	Game machines	Id card	Memory card solid state disk

Different types of memory cells are analyzed in digital VLSI. Each type of memory has its own special characteristics. In the analysis of low power circuits Memory circuits are very important . For example, DRAM is used in main memory and has features of high density and fast speed. Due to high speed SRAM is used as the cache memory. Drawback of volatile memory is that stored data in memory is lost when power is turned off, to overcome this problem ROM came into picture. Due to cost and reliability issues of EPROM, they have fallen out of favor and have been replaced by Flash Memories. NAND flash is used for data storage due to non-volatility and high density while NOR flash is used for code storage due to non-volatility and fast random access speed. So we can conclude that each memory cell has its own advantages and area in which it may be used.

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