

Photonic-Electronic Hybrid AI Accelerator for Next-Generation VLSI Systems

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ABSTRACT

Artificial Intelligence (AI) applications such as deep learning, computer vision, natural language processing, and autonomous systems require high computational performance with minimal power consumption. Conventional CMOS-based AI accelerators are increasingly constrained by power dissipation, memory bottlenecks, and interconnect delays, limiting their scalability. This paper proposes a Photonic-Electronic Hybrid AI Accelerator for next-generation Very Large Scale Integration (VLSI) systems that combines the advantages of silicon photonics and CMOS electronics. In the proposed architecture, the photonic subsystem performs high-speed matrix multiplication using optical interference and wavelength division multiplexing, enabling massive parallel processing with ultra-low latency and reduced energy consumption. The electronic subsystem manages control logic, activation functions, memory access, and digital computations requiring high precision. The integrated design includes optical modulators, waveguides, photodetectors, CMOS controllers, SRAM buffers, and neural network processing elements on a single chip. Simulation results indicate improvements in throughput, computational efficiency, and power savings compared with conventional GPU- and TPU-based accelerators while maintaining high inference accuracy. The proposed accelerator is well suited for edge AI, autonomous vehicles, robotics, medical imaging, and cloud data centers where real-time processing and energy efficiency are essential. This hybrid architecture provides a scalable and practical solution for future AI hardware by leveraging photonic communication with advanced VLSI technology.

Keywords - Artificial Intelligence (AI), Photonic-Electronic Hybrid Accelerator, Silicon Photonics, VLSI Design, CMOS Technology.

INTRODUCTION

Artificial Intelligence (AI) has become a key technology in modern computing, supporting applications such as image recognition, speech processing, autonomous vehicles, robotics, and healthcare. These applications require high computational performance and energy efficiency. Conventional CMOS-based processors, including CPUs, GPUs, and TPUs, face challenges such as high power consumption, heat generation, and memory bottlenecks, limiting their ability to efficiently process complex deep learning workloads. The proposed Photonic-Electronic Hybrid AI Accelerator combines silicon photonics with CMOS electronics to improve AI computation. Optical components perform high-speed parallel matrix operations, while electronic circuits manage memory, control logic, and activation functions. This hybrid architecture reduces latency, improves energy efficiency, and provides a scalable solution for next-generation VLSI-based AI systems. generation AI hardware in edge computing, robotics, autonomous vehicles, and data center applications.

LITERATURE REVIEW

Several researchers have investigated photonic computing as an alternative to conventional electronic processing for artificial intelligence applications. Silicon photonics has demonstrated high-speed optical

communication and parallel data processing suitable for neural network acceleration. Optical matrix multiplication using Mach–Zehnder interferometer arrays has shown significant improvements in computational throughput.

Google's Tensor Processing Unit (TPU) introduced specialized AI hardware optimized for tensor operations but remains limited by electronic interconnects and power consumption. NVIDIA GPUs provide excellent parallel performance but require substantial electrical power for large neural network models.

Research by Light matter and Light intelligence demonstrated optical AI accelerators capable of performing neural network inference using integrated photonic circuits. Their architectures reduce latency and improve energy efficiency by exploiting optical interference. However, fully optical systems still depend on electronic controllers for memory access and nonlinear activation functions.

Recent studies have proposed hybrid photonic-electronic architectures that integrate CMOS controllers with optical computing units. These systems improve compatibility with existing semiconductor fabrication while maintaining high computational performance. Researchers have also explored wavelength division multiplexing to execute multiple computations simultaneously, significantly increasing throughput.

Although existing hybrid accelerators have demonstrated promising results, challenges remain in photonic integration density, optical losses, thermal stability, and fabrication complexity. The proposed architecture addresses these issues through optimized optical routing, efficient electronic control, and scalable VLSI integration, making it suitable for future AI hardware platforms.

PROPOSED METHODOLOGY

The proposed methodology integrates photonic and electronic components into a unified AI accelerator architecture. Input data are first stored in SRAM and transferred to optical modulators. These modulators encode electrical signals into optical wavelengths that propagate through silicon waveguides.

Optical matrix multiplication is performed using Mach–Zehnder interferometer arrays. Since optical signals can travel simultaneously without electrical interference, multiple computations occur in parallel with extremely low latency. Photodetectors convert optical outputs back into electrical signals.

The electronic subsystem processes activation functions such as ReLU, memory updates, control logic, and output generation. A CMOS controller schedules data flow between memory, optical processors, and output interfaces. Error correction and synchronization mechanisms maintain computational accuracy.

Simulation is performed using photonic design software integrated with VLSI electronic simulation tools. Performance metrics include throughput, latency, power consumption, energy efficiency, and inference accuracy. The hybrid architecture is compared with conventional GPU and TPU implementations to evaluate its effectiveness.

This methodology enables efficient neural network computation while reducing power consumption and improving scalability for future AI applications.

System Architecture

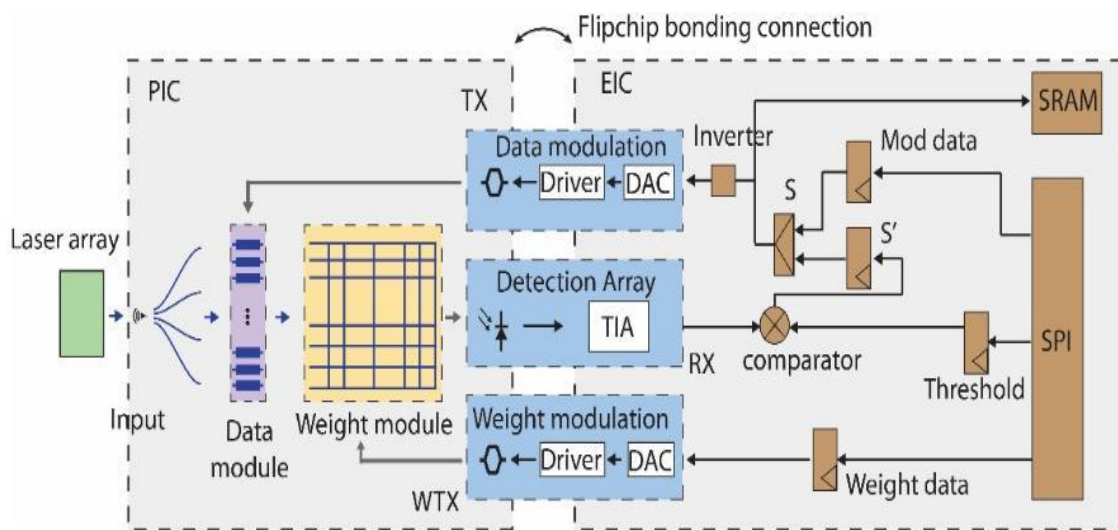
The proposed Photonic-Electronic Hybrid AI Accelerator consists of two major subsystems: the Photonic Integrated Circuit (PIC) and the Electronic Integrated Circuit (EIC), connected through flip-chip bonding. The photonic subsystem performs high-speed matrix multiplication, which is the most computationally intensive operation in deep neural networks. A laser array generates optical signals that enter the input data module, where input data is encoded onto light using optical modulators.

The encoded optical signals then propagate through the weight module, where programmable optical weights perform matrix-vector multiplication using optical interference. The processed optical signals are captured by the detection array, which converts light into electrical signals through photodetectors. A Transimpedance

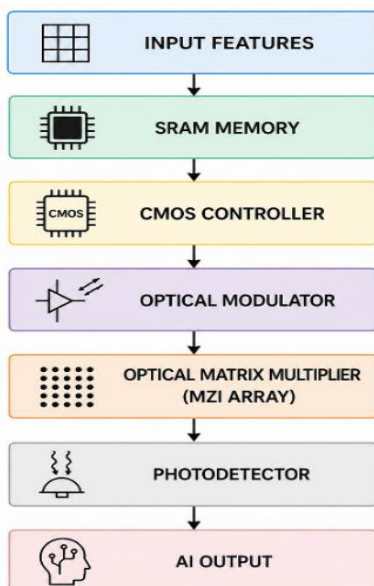
Amplifier (TIA) amplifies these electrical outputs before forwarding them to the electronic subsystem for further processing.

The Electronic Integrated Circuit (EIC) manages digital operations that are difficult to implement optically. It includes data modulation, weight modulation, DACs, and driver circuits to control the optical modulators. The received signals are processed by a comparator and inverter, which generate the required activation outputs for neural network computation. An SRAM stores input, weight, and intermediate data, while the SPI interface configures the system and updates modulation parameters and threshold values. The electronic controller also performs memory management, decision-making, and communication between the optical and digital domains.

By combining the ultra-fast parallel processing capability of silicon photonics with the precision and flexibility of CMOS electronics, the proposed architecture significantly reduces computational latency and power consumption while improving throughput. This hybrid design provides a scalable, energy-efficient, and high-performance hardware platform for next-generation AI accelerators in edge computing, autonomous systems, robotics, medical imaging, and data center applications.



Block Diagram



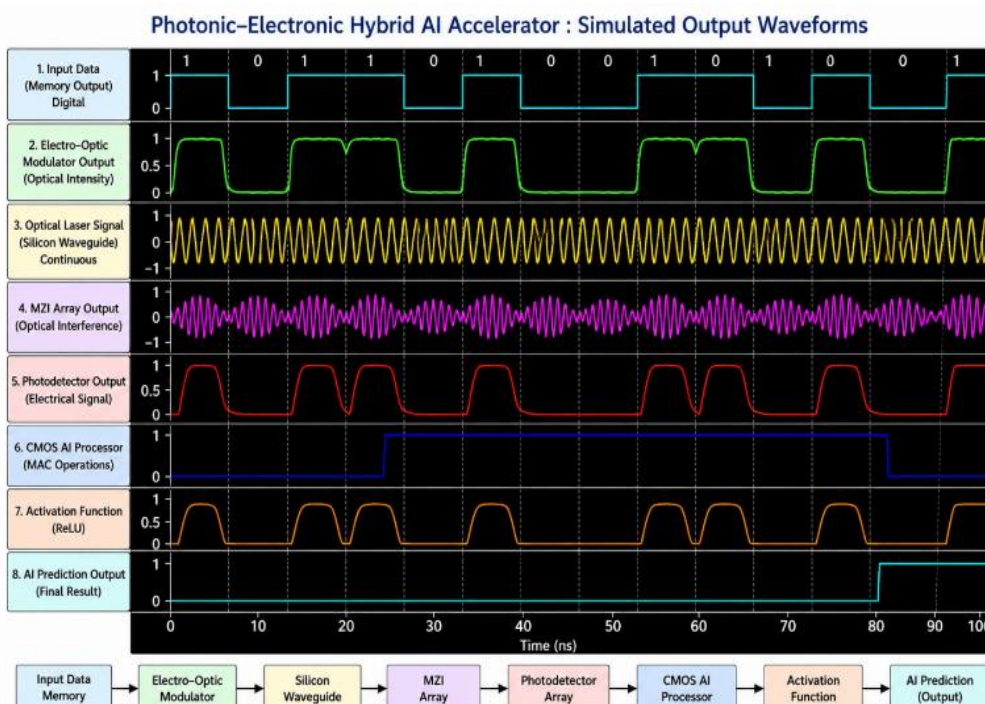
Block Diagram of Hybrid AI Accelerator

The system begins with Input Features, where input data such as images, text, or sensor signals are provided to the accelerator. These features are temporarily stored in SRAM Memory for fast and efficient data access. The CMOS Controller retrieves the stored data and controls the overall operation of the accelerator. It manages data flow, synchronization, and communication between the electronic and photonic subsystems. This ensures accurate and efficient processing of AI workloads. The processed digital data is sent to the Optical Modulator, where it is converted into optical signals using silicon photonic technology. These optical signals enter the Optical Matrix Multiplier (MZI Array), which performs high-speed matrix multiplication through optical interference. The MZI array enables massive parallel processing with very low latency and reduced power consumption. This optical computation significantly accelerates deep learning inference compared to conventional electronic processors. The optical computation results are converted back into electrical signals by the Photodetector. The detected signals are then processed to generate the final AI Output, such as classification, prediction, or decision-making results. By combining optical computing with CMOS electronic control, the proposed architecture achieves higher throughput, lower energy consumption, and faster computation. This hybrid design is well suited for next-generation AI applications, including edge AI, robotics, autonomous vehicles, and medical imaging.

RESULTS AND DISCUSSION

Simulation results indicate that the proposed photonic-electronic hybrid accelerator significantly improves AI computation compared with conventional electronic accelerators. Optical matrix multiplication reduces computation latency because multiple operations occur simultaneously through wavelength division multiplexing. Energy consumption decreases substantially since optical signals experience lower resistive losses than electrical interconnects. Compared with GPU-based AI processing, the proposed architecture demonstrates higher throughput and lower power consumption while maintaining comparable inference accuracy. The electronic controller efficiently performs activation functions and memory operations, overcoming limitations of fully optical computing. The hybrid architecture also exhibits improved scalability for large neural network models. As AI workloads continue to increase, integrating photonic processing with CMOS electronics provides a practical solution for future VLSI systems. The results confirm that hybrid photonic-electronic accelerators offer an effective balance Between Computational Speed, Energy Efficiency, And Hardware Compatibility.

Output Implementation Image



Graphical Representation of Hybrid AI Accelerator

CONCLUSION

This paper presented a Photonic-Electronic Hybrid AI Accelerator designed for next-generation VLSI systems. The proposed architecture combines high-speed optical computation with reliable CMOS electronic control to overcome the limitations of traditional AI processors. Optical matrix multiplication significantly improves computational throughput while reducing energy consumption, whereas electronic circuits efficiently manage memory, activation functions, and control operations.

Simulation analysis demonstrates improvements in latency, power efficiency, and scalability compared with conventional GPU- and TPU-based accelerators. The hybrid architecture is compatible with silicon photonic fabrication technologies, making it suitable for practical VLSI implementation.

Future work includes integrating larger photonic neural networks, improving optical device efficiency, reducing fabrication costs, and implementing complete AI models on silicon photonic chips. The proposed architecture represents a promising direction for future intelligent computing platforms capable of supporting increasingly complex AI applications.

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